DEGRADATION, RELIABILITY, AND FAILURE OF SEMICONDUCTOR ELECTRONIC DEVICES

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ABSTRACT

We show how defects in semiconductor device structures are formed, how they can affect the properties and reliability of devices, and how they might be avoided. Examples will be drawn from wide band gap semiconductor materials and devices we have fabricated in-house or examined for DARPA, collaborators in the P&E CTA, a power electronics MTO, or an SBIR.

Keywords: Wide band gap semiconductor device degradation, reliability, material device correlations

1. INTRODUCTION

Semiconductor devices are composed of metal contacts, dielectrics, and ceramic packages, as well as the semiconductor itself. Chemical impurities and the distribution of the dopants in the semiconductor can have a profound effect on how close the device can operate to its theoretical optimum performance level. Crystalline defects in the single crystal semiconductor can also degrade the properties of the device. How well the metal contacts adhere to the semiconductor surface affect the device reliability, and the resistance of the ohmic contacts determines to some extent the highest frequency at which the device can operate. The gate dielectric in a field effect transistor may also limit the ultimate operating frequency of the device, as well as its operating voltages. Current leakage through the dielectric degrades the device, and trapping of charge in it can cause the device properties to change over time. How well the device is bonded to the ceramic package determines its ability to conduct heat away that is generated by the operation of the device and therefore its operating temperature. The temperature at which the device operates in the steady state has profound effects on how well the device operates, as well as its reliability.

Because of its large band gap, reasonable electron mobility, and the fact its aluminum alloy has large piezoelectric coefficients, high electron mobility transistors (HEMT's) fabricated from gallium nitride (GaN) can generate four to five times the amount of power that a comparable gallium arsenide (GaAs) HEMT can (Wu, et al., 2004). Among other things, this can more than double the range of detection and/or target discrimination distance in the appropriate radar systems. Also, for the same power level it has an input impedance ten times that of a comparable GaAs HEMT which enables it to operate more efficiently over a wide band width. As shown in Fig. 1, one such application is for the Fire Finder radar system. All of the DoD labs, as well as DARPA, are aware of these facts, and so have invested heavily in this area. Although much progress has been made, GaN HEMT's are not yet available for use in military systems because they have still not reached their full potential, degrade over time, and are not reliable.

Fig. 1. A Fire Finder radar system that could operate more efficiently and have a wider bandwidth if GaN HEMTs were substituted for GaAs HEMTs.

This is due in large part to the poor quality of the GaN films used to fabricate the devices. It is poor because it is not yet possible to grow GaN substrates that are large enough and of suitable quality on which to grow the films. As a result, materials other than GaN have to be used as the substrate, which results in a large number of mismatch dislocations due to a difference in lattice parameters. We show how these defects are formed and how they can be measured and characterized using x-ray diffraction (XRD), transmission electron microscopy (TEM), and etch pit density (EPD) maps. The number and type of defects formed depend on how the films are grown, as well as the substrates on which they are grown. We show this by comparing films grown by the metal organic chemical vapor deposition (MOCVD) and molecular beam epitaxy (MBE) methods. We also show how the defects can increase the gate leakage and lower the transconductance, and are responsible for current collapse and the device properties changing with time.

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Even though SiC has a smaller electron mobility than GaN, much higher quality SiC is available for device fabrication. As a result, it is the preferred semiconductor for high power, high temperature applications such as those used in an inverter circuit in hybrid electric vehicles such as the one shown in Fig. 2. Its large energy gap, and therefore large breakdown field, enables it to perform more efficiently and faster than comparable devices fabricated from silicon (Cooper et al. 2002). The large energy gap also enables the devices to operate at temperatures higher than devices made from silicon thereby reducing, and in some cases eliminating, the need for heavy, noise generating cooling systems that consume valuable space. As good as the SiC material is, it still is not nearly as good as silicon so in many instances SiC devices are not yet ready to be inserted.

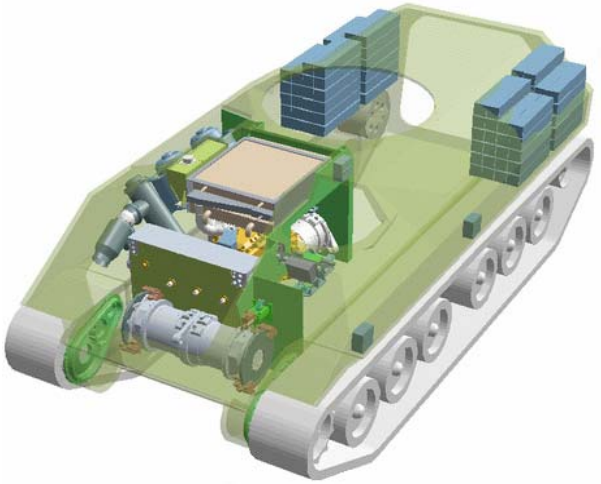


Fig. 2. Hybrid electric vehicle that will operate more efficiently and quietly when SiC devices are substituted for silicon devices in the inverter circuits.

One aspect of the problem is that the SiC substrates often contain too many crystallographic defects such as small angle grain boundaries and stacking faults. We show how we have identified them using XRD, TEM, and EPD maps. Further, we show these defects can propagate into the films and can degrade the operation of PiN diodes. SiC has the trait that it can appear in many different crystal structures known as polytypes. It is essential for only one type – preferably the 4H-polytype – to be present in the wafer for devices fabricated on it to work effectively. Unfortunately, SiC cannot be doped effectively by the in-diffusion of dopants. As a result, the dopants have to be ion implanted, and this process damages the SiC material. When the SiC is annealed to remove this damage, other polytypes can nucleate and grow causing the formation of stacking faults which negatively affect the device properties. Using TEM and an optical measurement technique called cathodoluminescence (CL), we show how this can occur. Ion implantation is often used to reduce the large electric fields at the edges of devices which can cause premature breakdown in the devices, but we show that the ion implantation process can also lead to premature breakdown. An alternative to the ion implantation process is regrowing heavily doped SiC in trenches that were patterned and etched using a tantalum carbide (TaC) mask. We show how this TaC mask can be deposited by pulsed laser deposition (PLD) and etched; we also show the quality of the interface of the regrown SiC and the original wafer. Another important factor is the quality of the SiC – silicon dioxide (SiO_2) interface because that can determine the quality of the operation of a metal-oxide-semiconductor field effect transistor (MOSFET) made using it. One of the many important parameters of this interface is how much carbon has diffused into it. We show how this can be studied using electron energy loss spectroscopy (EELS).

2. PROCEDURE AND DISCUSSION

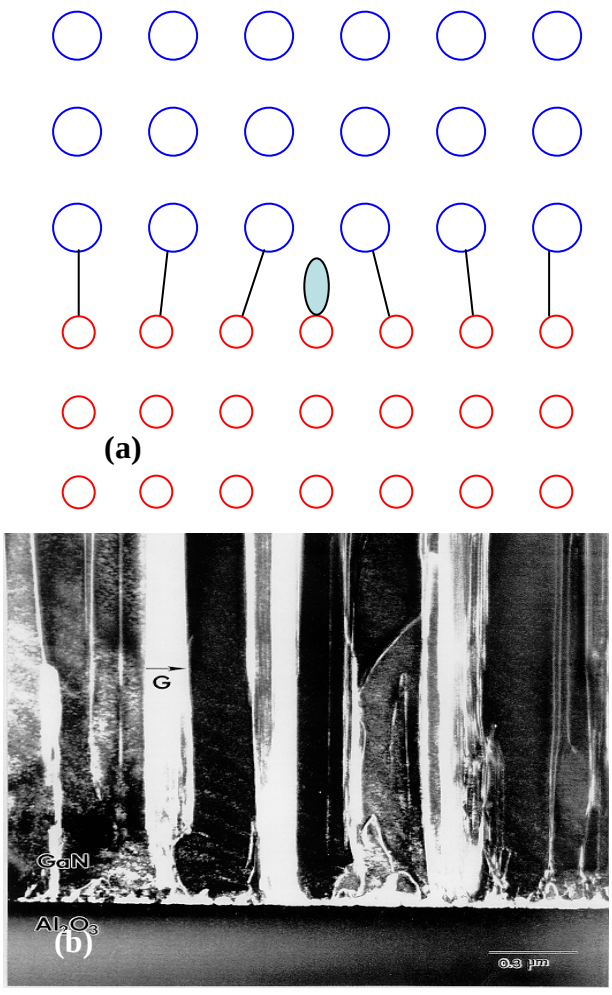


Fig. 3. (a) A schematic on how mismatch dislocations are formed. (b) TEM micrograph of the small angle grain boundaries formed in GaN grown on sapphire (Al_2O_3).

The primary reason the GaN films have so many defects is that the lattice parameter of GaN is different than

that of the substrate it is grown on. This is demonstrated schematically in Fig. 3a; the consequences of the GaN growing as filaments separated by small angle grain boundaries formed by large numbers of threading dislocations is shown in the TEM micrograph in Fig. 3b. One method for reducing the number of defects is a growth method called pendeo epitaxy. In this method a GaN film is deposited on a substrate such as sapphire or SiC, and then is patterned and etched to form parallel columns and channels with a specific crystallographic orientation. Under very specific MOCVD growth conditions growth occurs laterally from the columns out over the channels where two wings growing out in opposite directions from adjacent columns meet and coalesce. As shown in Fig. 4, these wings have many fewer defects because they are not forced to lattice match with the substrate. We show examples of materials that were grown by pendeo epitaxy (Zheleva et al., 1999), how the film can be processed so that devices are fabricated on the high quality wing regions, and how much better the material is in the winged regions as well as how much better devices fabricated in these regions operate (Zheleva et al., 2008).

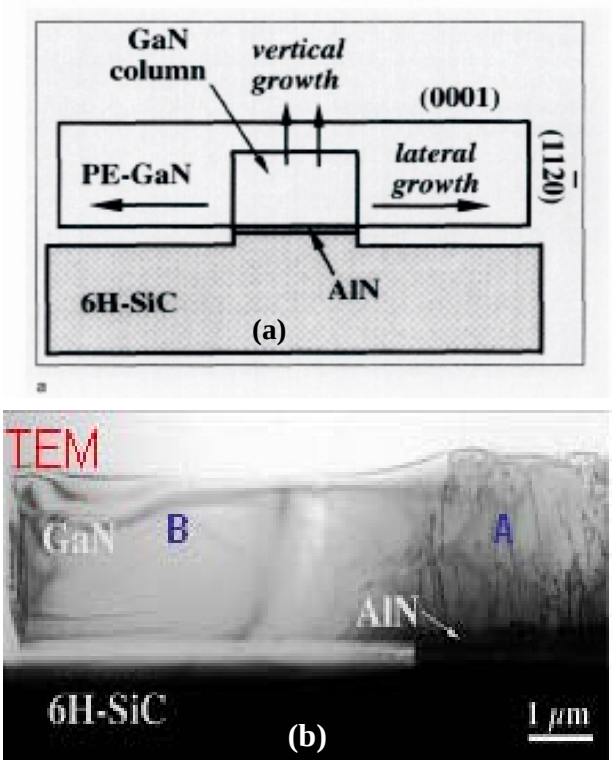


Fig. 4. (a) Schematic diagram demonstrating pendeo-epitaxial growth. (b) TEM micrograph of a pendeo film showing the more defective column **(A)** and more defect free wings **(B)**.

GaN HEMTs are required to have a thin (< 300 Å) AlGaN layer grown on them, and the devices will operate better when the surface is smoother. We found for one DARPA contractor that the channel mobility in their HEMTs, and therefore the transconductance, was smaller than expected because the surface had circular regions about 15 μm in diameter that were surrounded by what

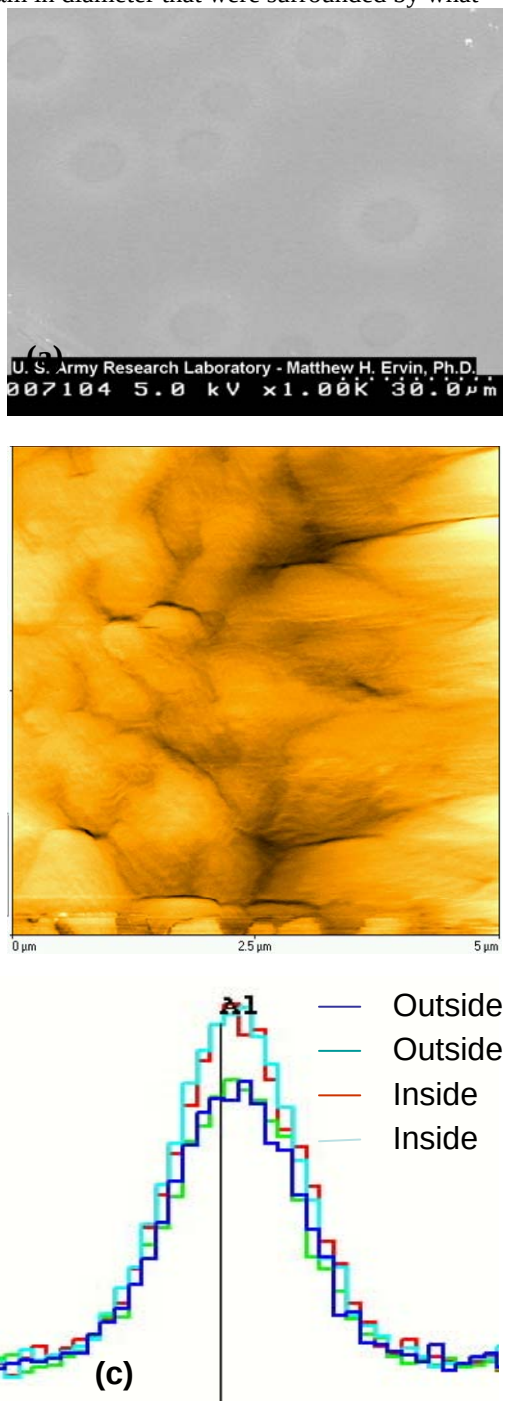


Fig. 5. (a) SEM micrograph of an AlGaN showing circular features. (b) AFM of a region near the edge of a circular region. (c) EDX of a region inside and outside of the circular regions.

appear to be pits, as is seen in the SEM micrograph in Fig. 5a. This result is confirmed in the AFM micrograph in Fig. 5b. Using an energy dispersive x-ray (EDX) attachment to the SEM, we found further that the Al concentration was not

everywhere the same, as it was larger inside the circular region. This is demonstrated in the EDX profiles in Fig. 5c. We concluded that this was a result of the temperature of the substrate in the MBE system was too low so that atoms that struck the surface did not have the energy to surface diffuse to their equilibrium positions. When the growth temperature was raised, the device properties were greatly improved.

It is generally known that if you can increase the Al content in the AlGaN, you can increase the number of charge carriers in the channel and therefore the peak power output of the device. However, when you increase the Al content, you also increase the mismatch strain between the AlGaN and the GaN, and once you reach the critical thickness limit, cracks will form in the AlGaN. We were able to determine the Al content in the AlGaN, using the θ-2θ x-ray curves like the one shown below in Fig. 6a, from the position of the AlGaN peak relative to the SiC substrate and GaN film peaks.

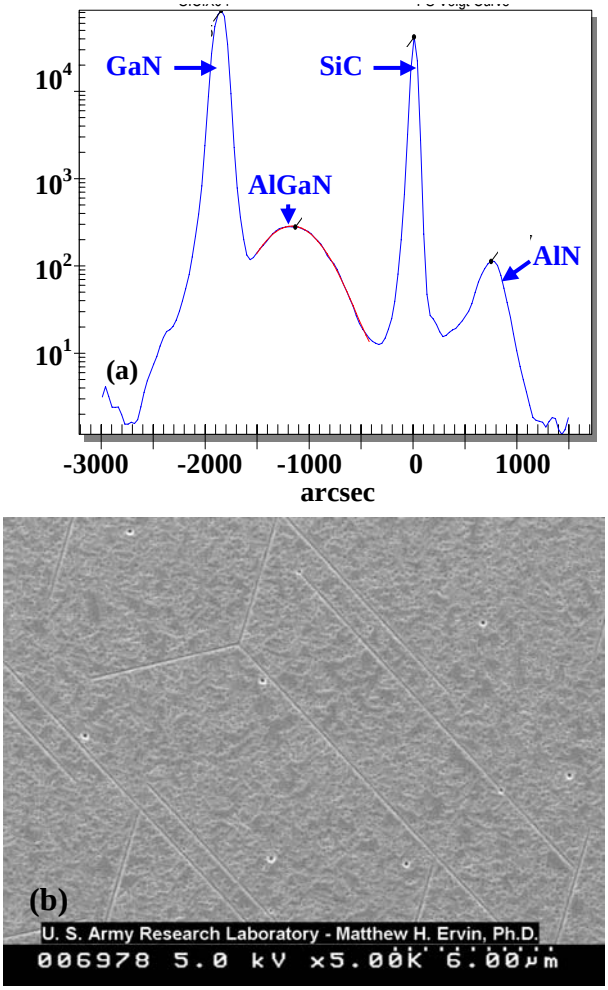


Fig. 6. (a) X-ray θ-2θ map used to determine the Al content in AlGaN. (b) Cracking in the AlGaN layer due to too much Al in the AlGaN.

When the films are grown, the surface has to be properly prepared and the sample cannot be cooled done too fast, or there will be a considerable amount of bowing created by the difference in the thermal coefficients of the film and substrate. One DARPA contractor was having problems with breakage and with processing the devices. Using our laser light scanner (LLS), we demonstrated that their wafers were highly bowed; an LLS simply records the reflected beam as a laser is scanned across the diameter of a wafer. As shown in Fig. 7, the wafer was so highly strained, it has a bowl shape with the edges of the bowl being as much as 45 µm lower than the center of the wafer. This is more than 10X the amount of bow we saw in good samples. After being advised of this, the contractor changed the way they deposited the AlN buffer layer in their MBE grown GaN HEMT structure and cooled down the sample more slowly after the growth was complete. The yield and the operation of the devices made from this structure improved significantly after these changes were made.

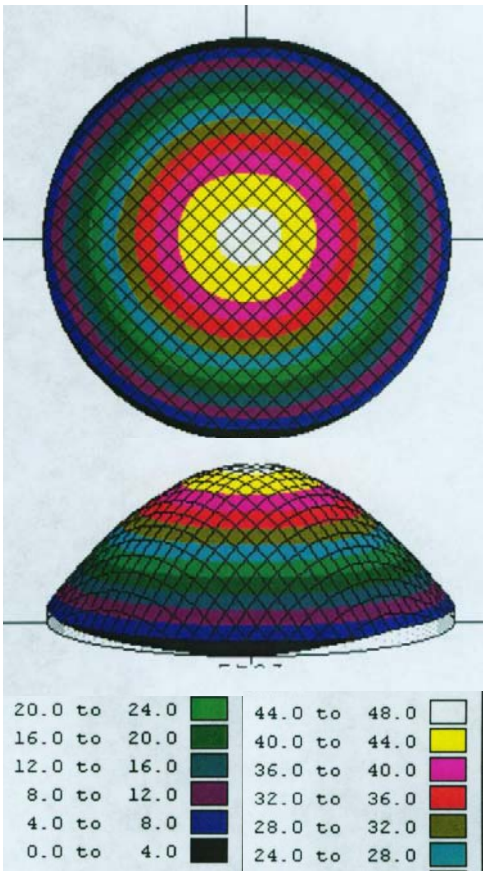


Fig. 7. Two and three dimensional views of a laser light scan of a highly bowed SiC wafer with an MBE grown GaN HEMT structure grown on it.

The distribution of impurities in the grown material is as important as its crystalline quality. One such example is that people have attempted to create a GaN 'substrate' by growing a very thick film of GaN on a silicon substrate using a technique called hydride vapor phase epitaxy

(HVPE), and then etching off the silicon. Although these 'substrates' are quite highly defective, they still have many fewer – about three orders of magnitude – dislocations. However, it is difficult to grow them pure enough so that they can have the required resistivity for operating at RF frequencies. One method to try to overcome this problem is to dope the films with iron, which creates states near the middle of the energy gap that can trap electrons thereby making the GaN 'substrate' more resistive. It is, however, difficult to incorporate the iron and have it be electrically active. Our SIMS profile showed that the Fe concentration oscillated out of phase with the O concentration, which is displayed below in Fig.8, as opposed to being constant. Work is on-going in learning how better to incorporate the Fe, but it is believed this interaction between the Fe and O is playing a critical role.

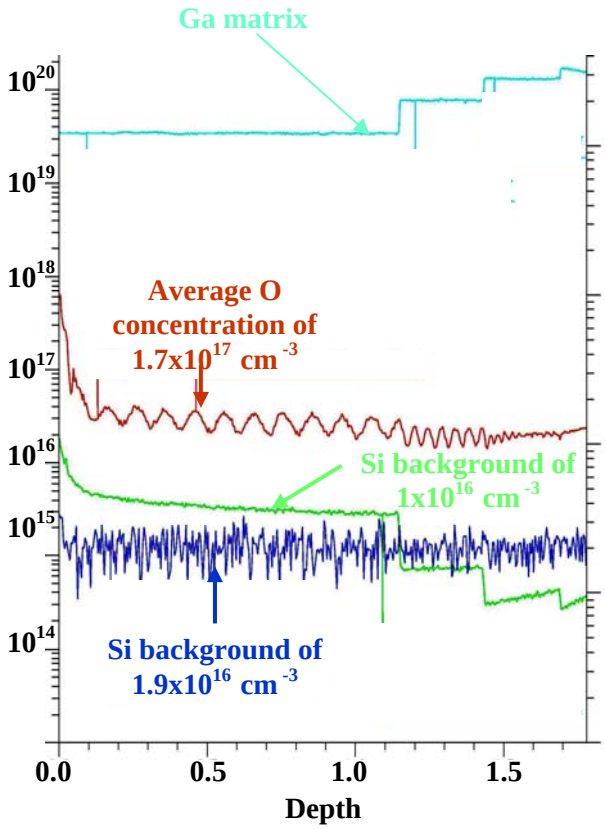


Fig. 8 SIMS profile of an HVPE GaN 'substrate' showing that the oxygen concentration oscillates as a function of the depth into the 'substrate'.

It is virtually impossible to dope SiC by thermal diffusion because the diffusion coefficients of the dopants are too small, even at temperatures as high as 1800ºC. As a result, the dopants have to be implanted. Initially, the dopants are not electrically active because most of them do not occupy the appropriate atomic site. Moreover, the lattice is damaged by the implants, and it has to be annealed out while at the same time the dopants diffuse to their equilibrium positions. Unfortunately, at the temperatures which this occurs, the silicon evaporates preferentially. We have pioneered the use of an AlN annealing cap that protects the surface during the anneal and can be etched off selectively using a warm KOH

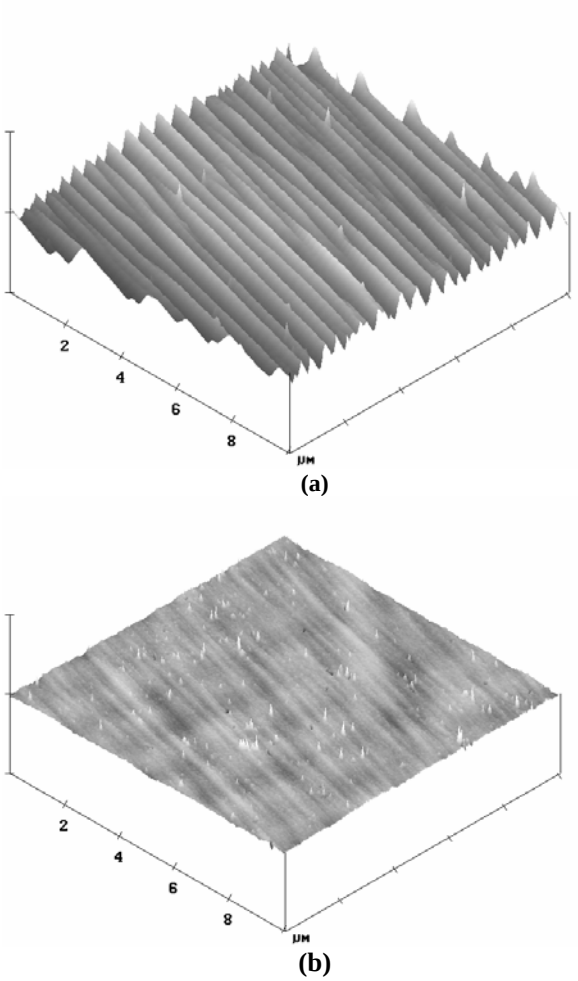


Fig. 9. AFM of the surface of a SiC film annealed at 1600ºC (a) without, and (b) with an AlN cap.

solution (Jones et al., 1999). As shown in Fig. 9, the surface annealed without the cap is much rougher. It is also likely that there are fewer silicon vacancies, which are electrically active, near the surface of the capped sample. This could be particularly important if MOSFETs were going to be fabricated on this sample because the current in these devices is carried near the surface. The rough topography of the unprotected surface would be more prone to scattering the electrons thereby reducing their mobility, and the vacancies could trap out some of the electrons thereby reducing the carrier concentration.

As shown in Fig. 10, the AlN cap has an upper limit, because it begins to noticeably evaporate at temperatures above 1600ºC. As a result, hexagonal etch pits are formed in it that expose the underlying SiC. To enable us to reach higher temperatures – temperatures at which a greater percent of the aluminum acceptors would be activated – we deposited BN on top of the AlN; we essentially capped the

cap (Ruppalt et al., 2003), as BN has an even lower vapor pressure than AlN. The BN was then removed by ion milling, and again the AlN was etched off chemically in warm KOH. The BN could not be put directly on top of the SiC because it cannot be chemically removed, and if it were removed by ion milling, the ions would simultaneously damage the SiC surface.

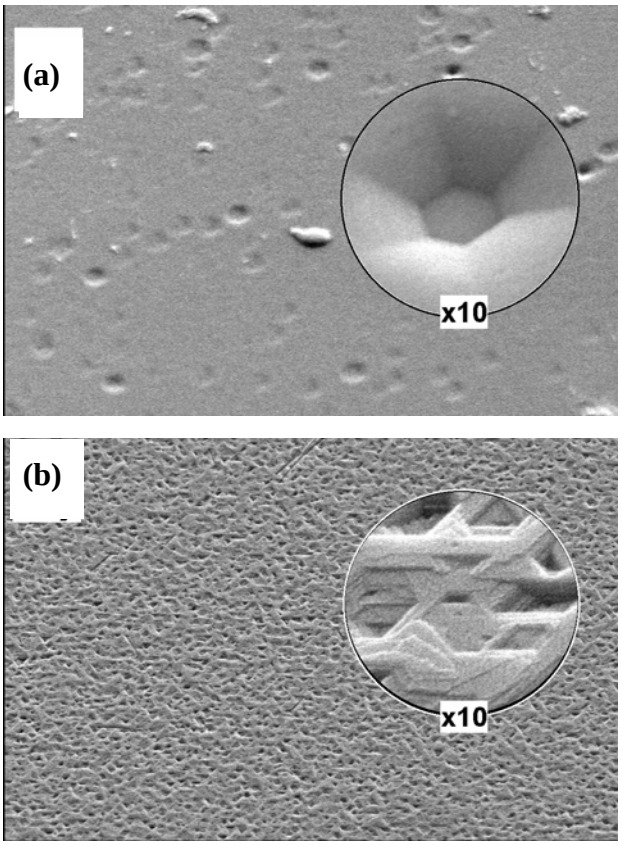


Fig. 10. SEM micrographs of an AlN cap heated to (a) 1650ºC or (b) 1700ºC for 30 min.

Though we are now able to anneal the implanted SiC up to temperatures as high as 1800ºC, we have determined that even at this high temperature, all of the defects cannot be annealed out. In fact, some defects appear to nucleate and grow. We believe that stacking faults have formed, which means that there are small regions that no longer have the desirable 4H-SiC crystal structure; rather there are small islands of SiC that have the 3C- or 6H-SiC structure. Having different phases present is detrimental because they scatter the electrons thereby increasing the resistance. It is also likely they create states in the energy gap that can act as carrier traps as is represented by the D_I defect that always seems to be present in ion implanted SiC (Jones et al., 2004a, 2004b). (Storasta et al., 2001) believe that this defect is a deep donor capable of trapping out aluminum acceptors. We have suggested that these stacking faults are created by the condensation of silicon – carbon divacancy pairs (V_{Si}-V_C) which form Frank intrinsic stacking faults. As seen in Fig. 11, these stacking faults not only grow in size, but they also appear to migrate towards the surface. This could be detrimental to MOSFETs, which, as stated before, have currents that flow very close to the surface. We are presently looking at ways to overcome this problem by growing a thin epitaxial layer to cover the implanted region thereby keeping the current flow away from the persistent ion implanted defects. Working with RPI, we are also attempting to replace ion implanted regions with regions that are selectively grown. For example, the ion implanted regions of the JBS diode shown in Fig. 12 could be replaced by growing p+ layers in the channel while protecting the columns from being grown on by protecting them with a TaC cap.

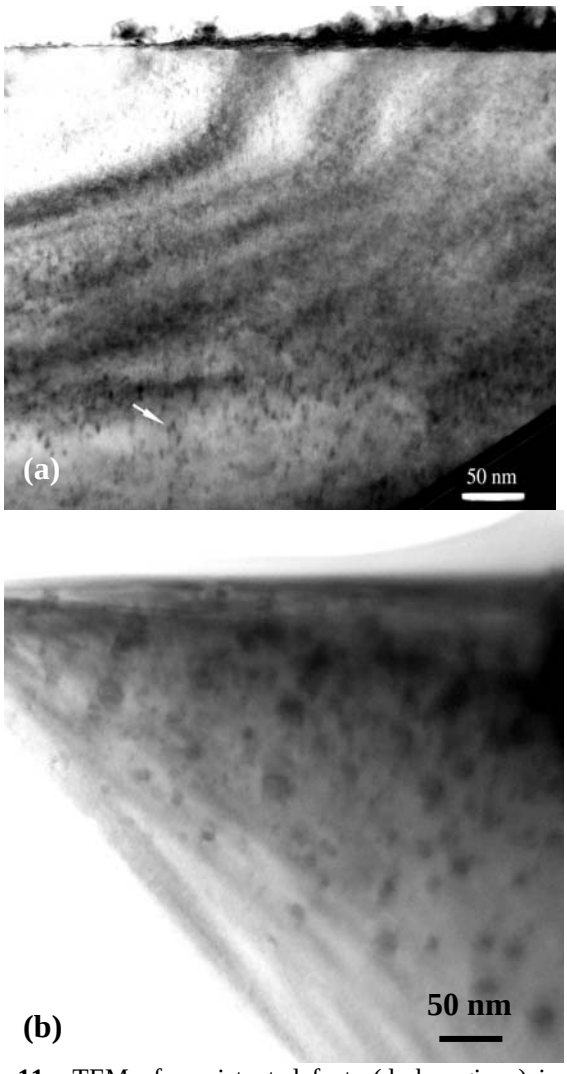


Fig. 11. TEM of persistent defects (dark regions) in ion implanted 4H-SiC annealed at (a) 1600 and (b) 1700ºC.

This knowledge was used to improve the quality of the JBS diode shown in Fig. 12. The theory behind this diode is that it combines the best properties of Schottky barrier and PiN diodes. The former has a lower resistance when operating under forward bias, so the current flows from the

Schottky metal to the n-SiC. The latter has a lower reverse saturation current and a larger breakdown voltage under reverse bias, so the p+ regions are located close enough to each other so that their depletion layers overlap under reverse bias forcing the current to flow from the p+ to the n-SiC. From theoretical considerations, one should dope the p+ regions as heavily as possible. However, because the p+ region was implanted, it contains a number of persistent defects, and these defects do the most damage to the properties of the diode when they are located close to the p-n junction. It is also the case that the more heavily doped material contains the largest number of these defects. Thus, a compromise was made to reduce the concentration of the implanted ions near the p-n junction, but retain the high concentration of implanted ions away from the junction where the higher doping levels outweighed the negative effects of the persistent defects. Thus, as shown in Fig. 12b, the region implanted near the junctions was implanted with 10^{19} cm^{-3} Al, while the region away from the junction was implanted with 10^{20} cm^{-3} Al. Clearly, the more heavily doped region contains more damage.

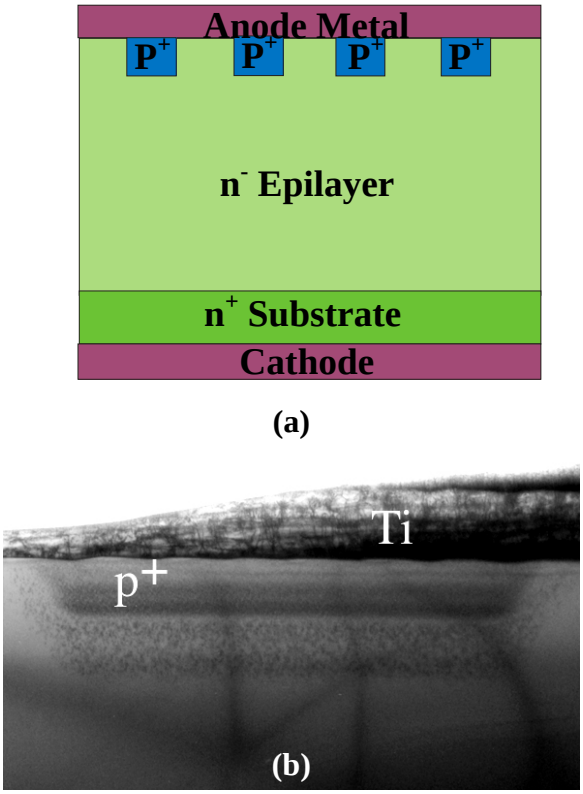
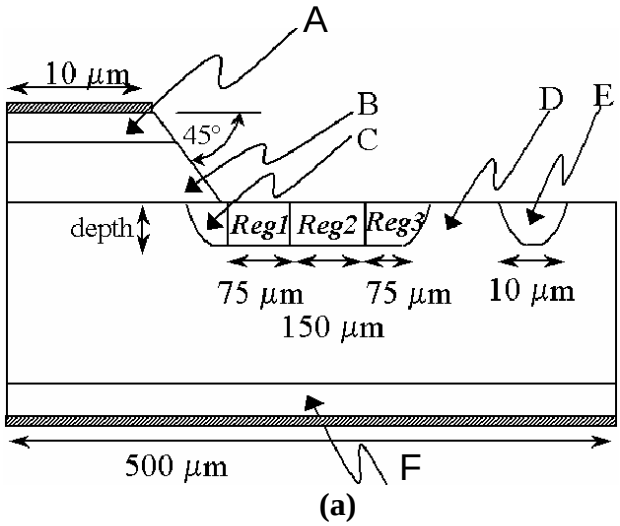


Fig. 12. (a) Schematic of a JBS diode, and (b) TEM of of an ion implanted p+ channel with the higher concentration, and therefore the damage, being larger in the p+ region. The Ti metal can form a Schottky contact.

The persistent ion implant damage is not limited to the active device, as it can also affect the ability of guard rings implanted around the device to reduce the electric field at the edges of the device to help prevent premature breakdown. This is displayed in Fig. 13a. One problem we believe this causes is that the implants can themselves contribute to the breakdown. This is suggested by the microplasmas, point sources of light emission, that occur when the diodes breakdown prematurely. We speculate that the light is produced when recombination occurs at the defect sites. We attempted to prove this by using a FIB to cut out parts of the sample in the regions where the microplasmas occurred, and to look for them in the TEM, but currently the results are inconclusive. This is a very difficult challenge, as it is like looking for a needle in a haystack. The samples are a few microns in diameter, whereas the defect we were looking for is probably only a few nm in size.



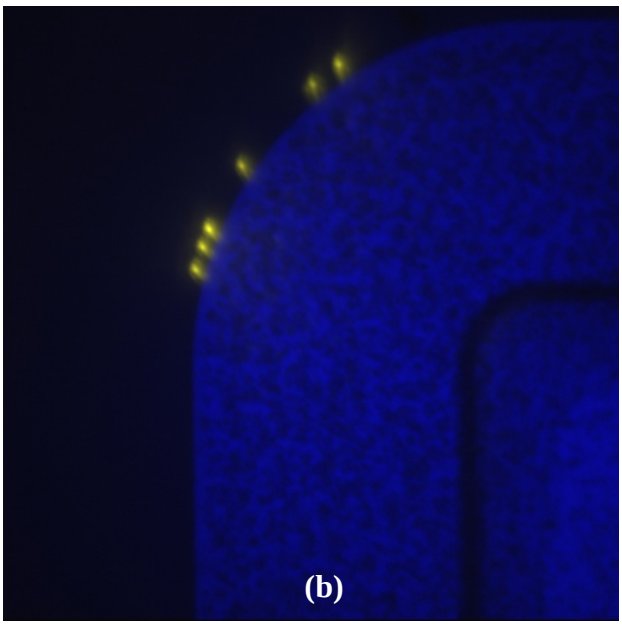


Fig. 13. (a) Schematic diagram of a JBS diode showing implanted guard rings in regions 1 2 & 3.(b) Microplasmas created during premature breakdown that could be created by recombination of charge carriers at a persistent ion implanted induced defect.

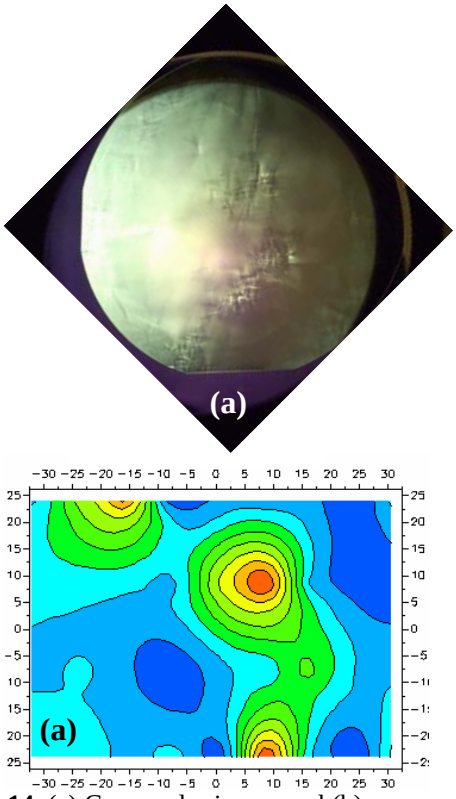


Fig. 14. (a) Cross polar image and (b) x-ray rocking curve map of a SiC wafer showing correlations between the two types of measurements.

Another project we have begun is to attempt to trace the formation of defects in a wafer from the beginning and how they ultimately affect the properties of the devices made from it. A quick method for assessing the quality of a wafer is to examine it in a crossed polar microscope (Fig. 14a). Light passing through the wafer is affected by strains in it thus marking some of its strain fields. One can see there appears to be a line of defects starting to the left of center at the bottom, moving up towards the middle, and veering to the left. A more sophisticated, but more time consuming method for examining these strain fields can be done by plotting the width of an x-ray rocking curve determined at various locations on the wafer and plotting them on a 2D map where the blues represent a narrow rocking curve and the reds represent wider ones (Fig. 14b). One can see that the two figures have similar patterns. Other experiments being done in this effort, but there is not room to describe them here, are x-ray topographs taken with synchrotron radiation that mark out the dislocations and small angle grain boundaries, maps of defects called micropipes, and x-ray peak position maps and LLS's that describe how the crystal planes and wafer are bent. Defects in films grown on these wafers are also being recorded using the same set of techniques, and ultimately PiN diodes will be made on these wafers and the characteristics of devices from different parts of the wafer will be compared with these defect maps.

Summary

The properties of semiconductor devices can be diminished by crystalline defects and chemical impurities introduced during the growth of the device structures and/or while the devices are being fabricated. These defects can also lessen the reliability. Using wide band gap semiconductor devices made from GaN and SiC, we have shown why some devices did not operate as well as they should or failed prematurely, or why the device yield was low. HEMT's for high power, high frequency applications such as radar made from GaN were shown in one case to have a non-uniform distribution of aluminum in the AlGaN layer, in another to have a surface that was too rough, in another to have too much aluminum in the AlGaN layer, and in still another to have buffer layers that were not properly prepared. SiC devices used for high power applications such as in hybrid electric vehicles were shown to have ion implanted induced defects that can cause higher reverse saturation currents and premature breakdown in diodes. They also can decrease the gain in transistors and increase their forward resistance. In addition to examining devices made by others, we fabricate devices from materials that have been completely characterized by us in order to obtain a better understanding of how these defects affect the device properties and contribute to their reliability and/or failure.

References

Cooper, J.A., Melloch, M.R., Singh, R., A. Agarwal, A. and J.W. Palmour, 2002, IEEE Electron Devices., **49** , 658.

Jones, K.A., Shah, P.B., Kirchner, K.W., Lareau, R.T., Wood, M.C., Ervin, M.H., Vispute, R.D., Sharma, R.P. Venkatesan, T., and Holland, O.W., 1999, Mater. Sci. and Eng., **B61-62,** 281.

Jones, K.A., Derenge, M.A., Ervin, M.H., Shah, P.B., Freitas, J.A., Vispute, R.D., Sharma, R.P., and Gerardi, G.J., 2004a, Physica Status Solidi, Vol**. 201A**, 496.

Jones, K.A., Shah, P.B., Zheleva, T.S., Ervin, M.H., Derenge, M.A., Freitas, J.A., Harmon, S., McGee, J., and Vispute, R.D., 2004b, J. Appl. Phys., **96**, 5613.

Ruppalt, L.B., Stafford, S., Yuan, D., Jones, K.A., Ervin, M.H., Kirchner, K.W., Zheleva T.S., Wood, M,C., Geil, B.R., Forsythe, E., Vispute, R.D., and Venkatesan, T., 2003, Solid State Electron, **47**, 253.

Storasta, L., Carlsson, F.H.C., Sridhara, S.G., Bergman, J.P., Henry, A., Egilsson, T., Hallen, A., and Janzen, E., 2001, Appl. Phys. Lett., **18**, 46.

Wu,Y.-F., Saxler,A., Moore,M., Smith,R.P., Sheppard, S., Chavarkar, P.M., Wisleder, T., Mishra, U.K., and Parikh, P., 2004, Electron Dev. Lett., **25**, 117.

Zheleva, T.S., Ashmawi, W.M., and Jones, K.A., 1999, Phys. Stat. Sol., **176**, 545.

Zheleva, T.S., Derenge, M.A., Jones, K.A., Shah, P.B., Molstad, J., Lee, U., Stepp, 2008, to be published in Proceedings of the Army Science Conf., Nov. 2006.

Degradation, Reliability and Failure of Semiconductor Electronic Devices

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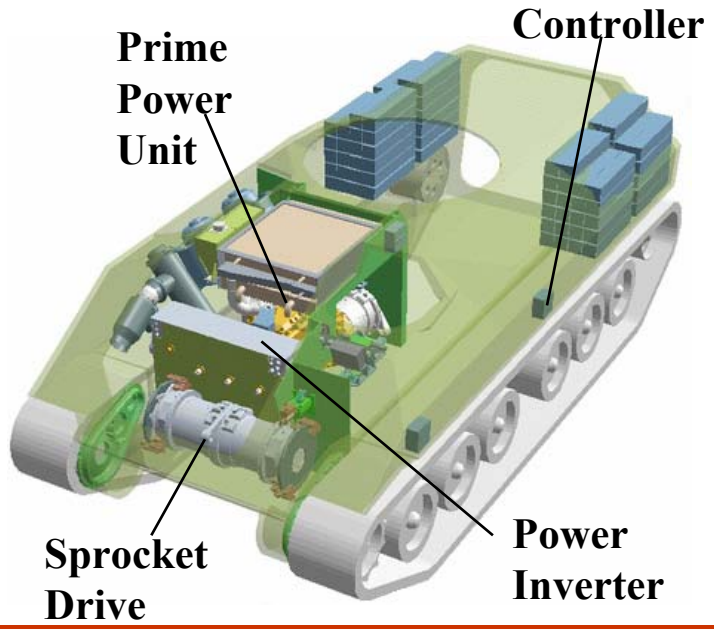
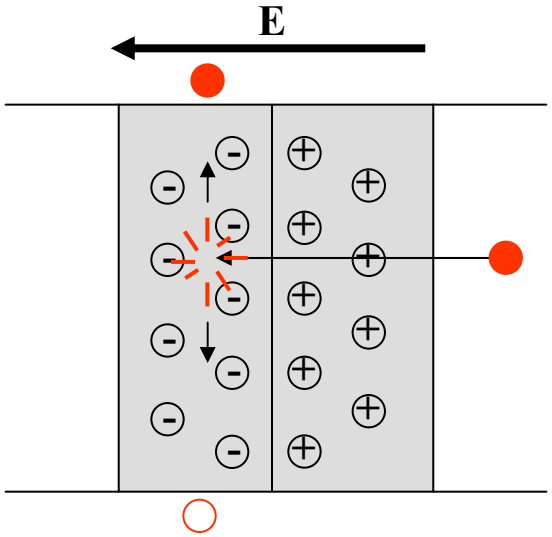
Potential Applications for Wide Bandgap (WBG) Semiconductors

A Fire Finder radar system that could operate more efficiently and have a wider bandwidth if GaN HEMTs were substituted for GaAs HEMTs.



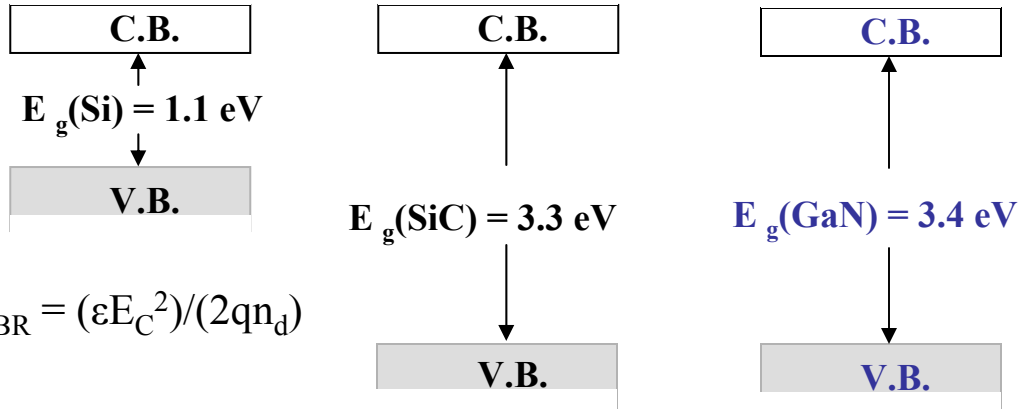
A Hybrid Electric Vehicle that could operate more efficiently, be more stealth, and have electronics that take up less space if SiC diodes and transistors were substituted for those made from Si.

WBG Semiconductors Can Handle More Power and Operate at Higher Temp.



Avalanche Breakdown

1. Relatively large breakdown voltage, V_{BR}
   a. Electric field at junction cannot exceed E_C
   b. E_C ten times larger in SiC than in Si
   c. E_C ten times larger in GaN than in GaAs
2. Want to be able to operate at higher Temp.
   a. Want to cool SiC devices with engine oil
   b. Eliminates noisy, large volume cooling app.
   c. With small E_g Si cannot operate with T>150ºC
   d. Gate lengths for HEMTs < 0.2 µm
   e. High power density for short gate devices.

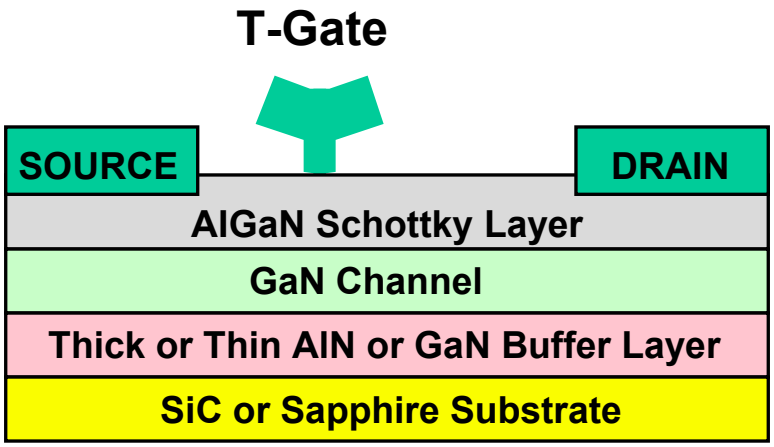


$V_{BR} = (\varepsilon E_C^2)/(2qn_d)$

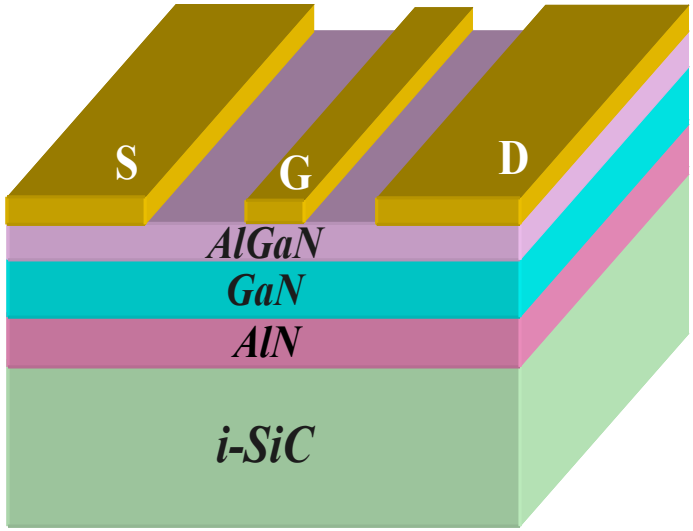
Energy Gap of Si, SiC and GaN

In addition GaN can produce blue light.

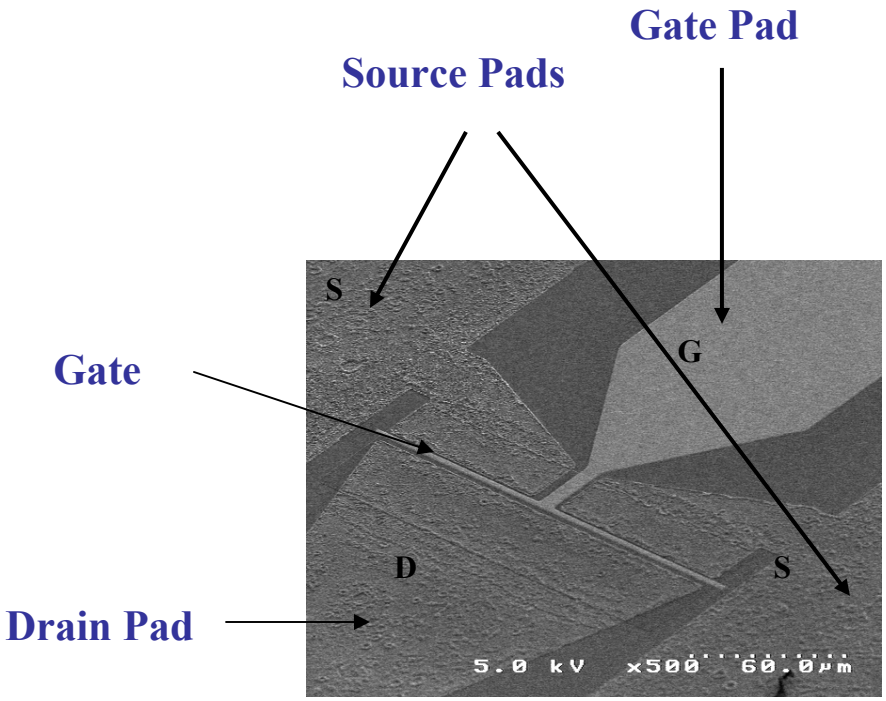
GaN/AlGaN HEMT



Side View of HEMT

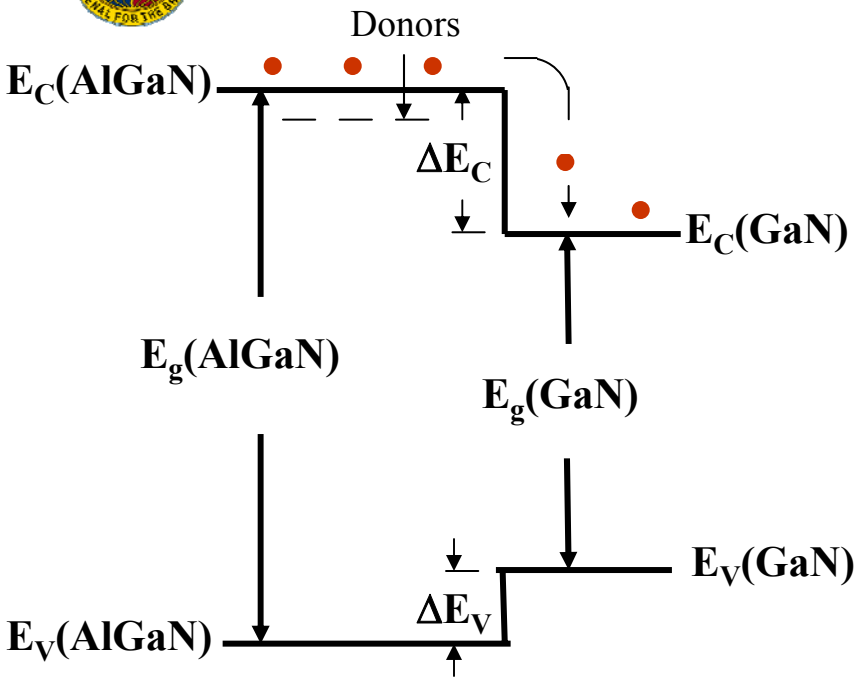


3D View of HEMT

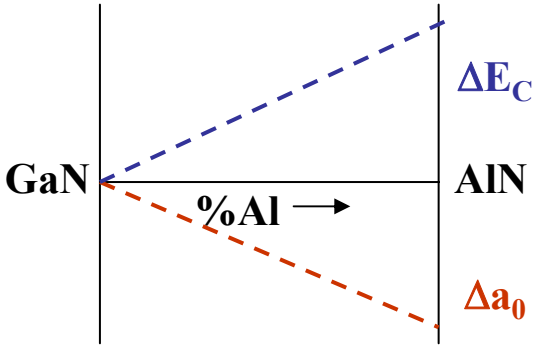


Perpendicular gate pad GaN/AlGaN HEMT

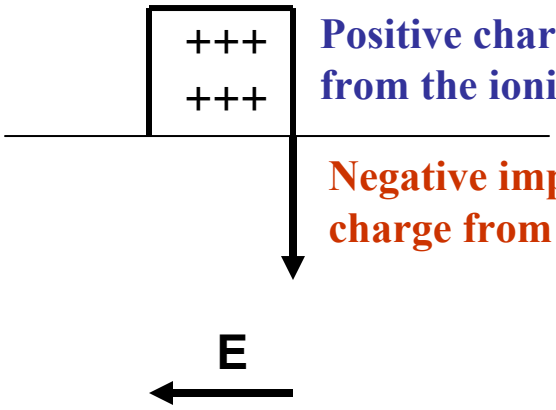
How A HEMT Operates - ΔE_g



AlGaN/GaN Band Energy Diagram



1. More Al, larger ΔE_C - good
2. More Al, larger Δa_0 - bad

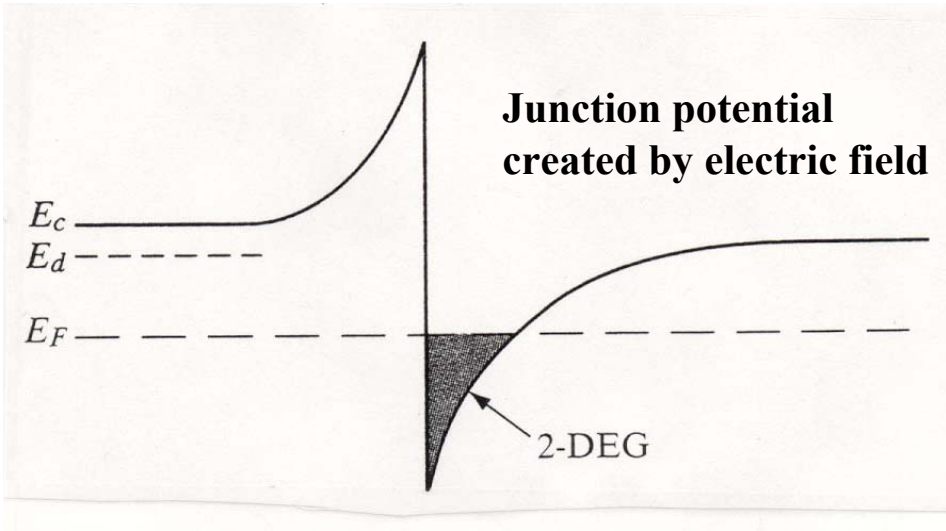


Positive charge in the AlN from the ionized donors

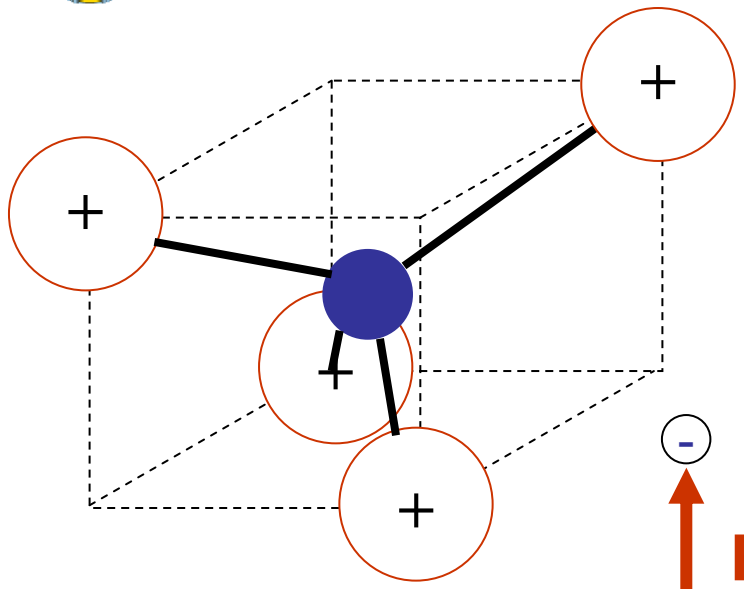
Negative impulse of charge from the 2DEG

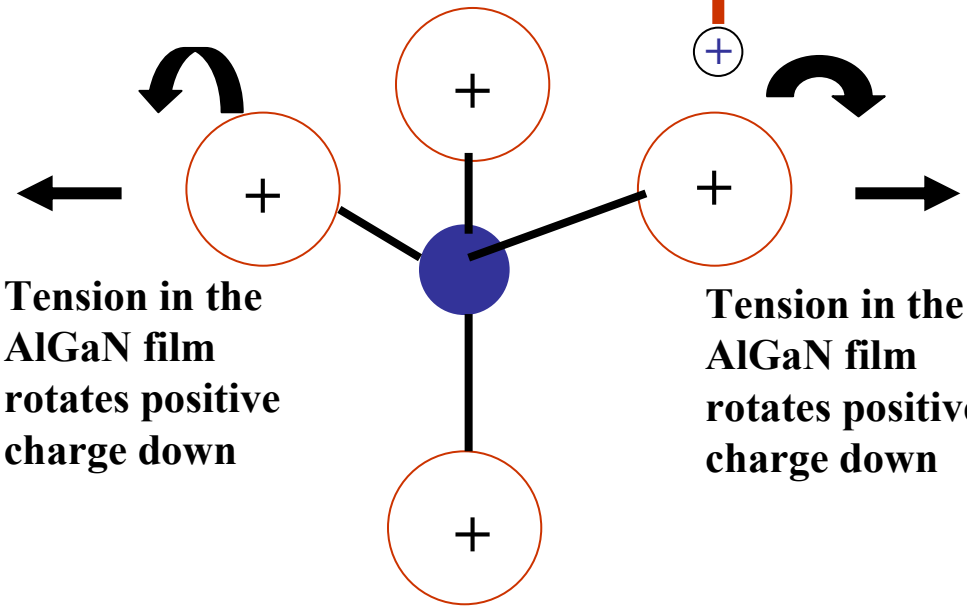
E

Internal electric field created by the charge separation



How A HEMT Operates - Polarization

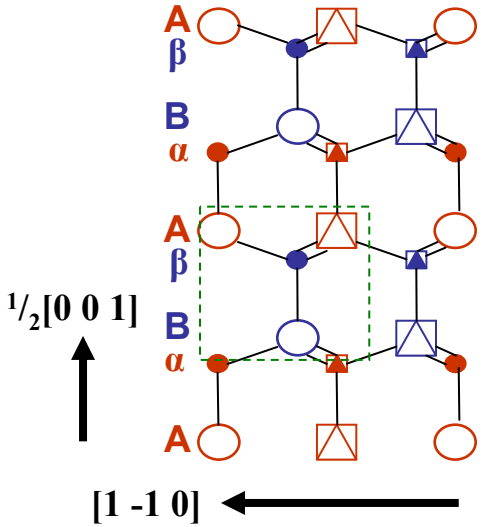




Tension in the AlGaN film rotates positive charge down

Tension in the AlGaN film rotates positive charge down

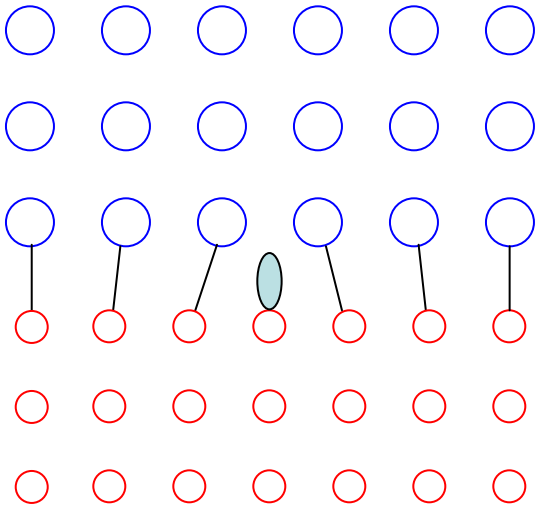
Most semiconductors have the sp^3 structure that form '3-legged chairs'. The Ga 'chair' is upside down, and the N chair is right side up. This makes semiconductors piezoelectric.



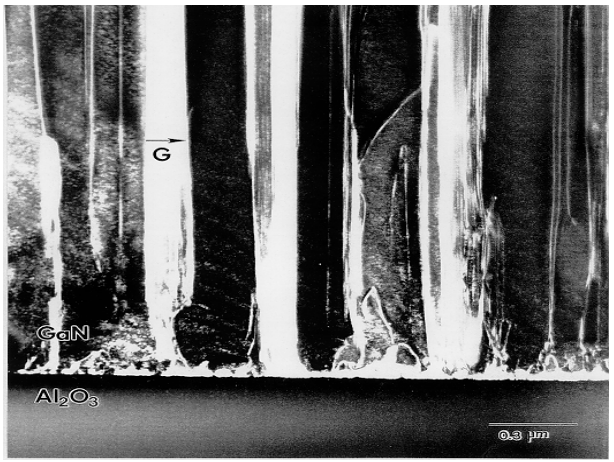
(110) Planar view of the wurtzite structure; the atoms in the green box form an sp^3 unit.

1. The AlGaN film has a smaller a_0
2. This puts the AlGaN film in tension
3. This produces + interface charge
4. Electrons attracted to plus charge
5. This increases the current density
6. More current, more power.

Effects of Lattice Mismatch



Mismatch produces dislocations

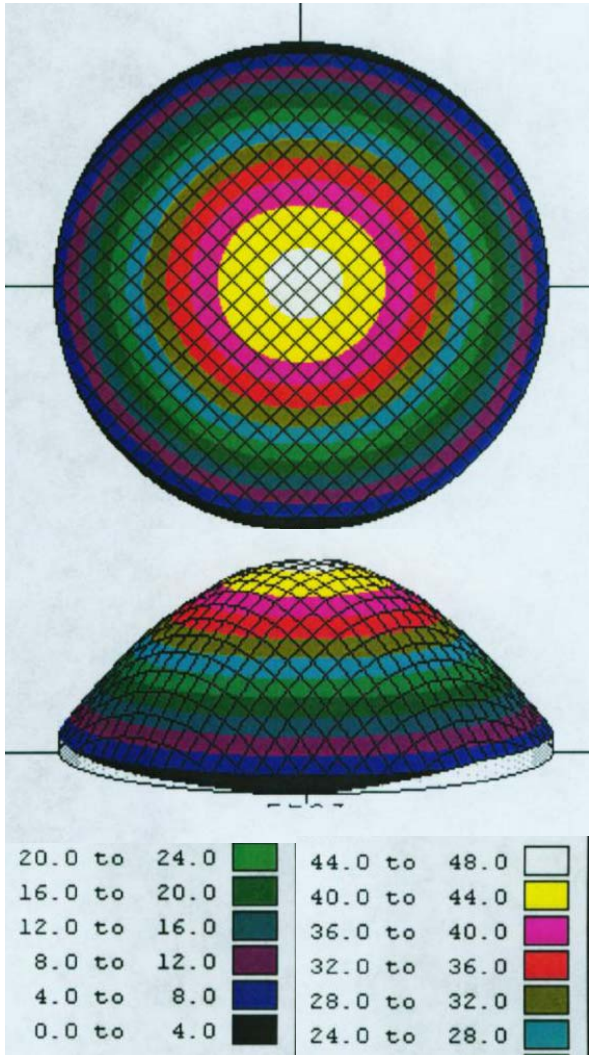


Acicular grains form during growth

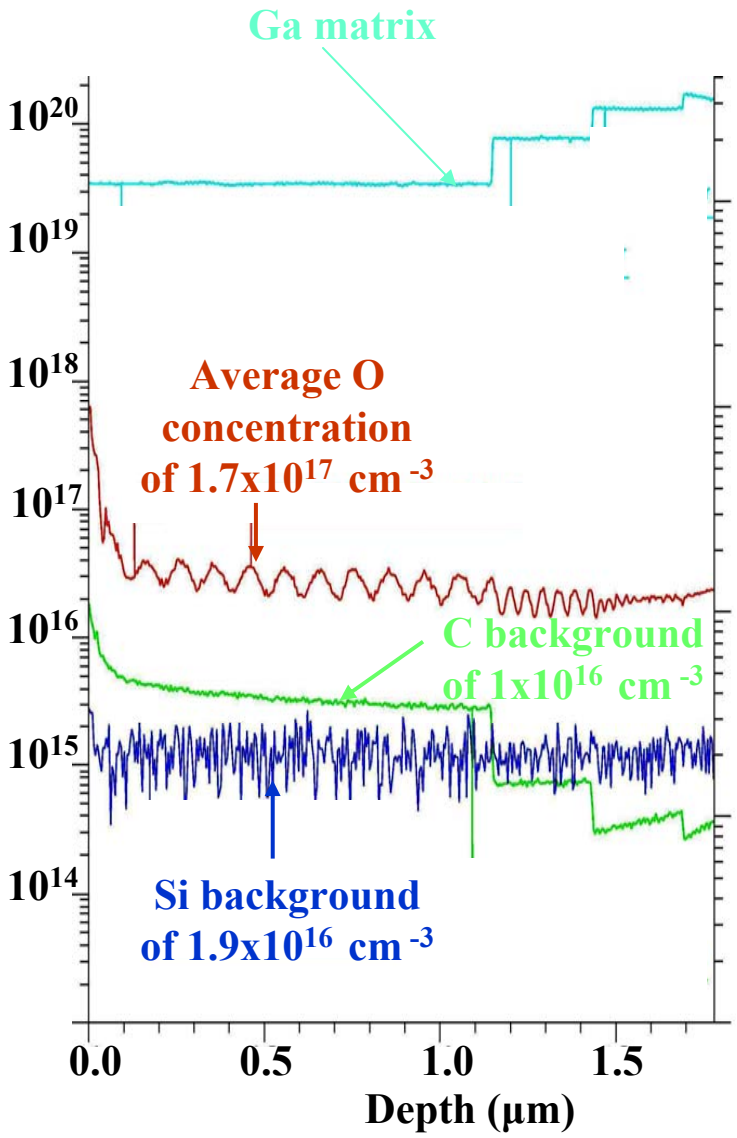
Substrate	Sapphire (Al_2O_3)	6H-SiC	ZnO or AlN	LAO, LGO $Li[Al(Ga)]O_2$	GaN
Lattice Mismatch (*a*-axis)	14%	3%	~2%	1.4%, 0.18%	0%
Crystal Structure	Hexagonal (Spiral Structure)	Hexagonal (Polytype)	Hexagonal (Perfect Wurtzite)	Tetragonal, Ortho-rhombic	Hexagonal (Perfect Wurtzite)

1. **GaN substrates cannot now be grown – it sublimates; all other substrates have a different lattice parameter.**
2. **This causes mismatch dislocations to form; their dangling bond structures are electrically active.**
3. **GaN films are not single crystal; they are composed of *c*-oriented, acicular grains separated by grain boundaries.**
4. **These small angle grain boundaries can be described by threading dislocations that are also electrically active.**
5. **Growth on foreign substrate requires low-T buffer layer.**

Problems in the Buffer Layer



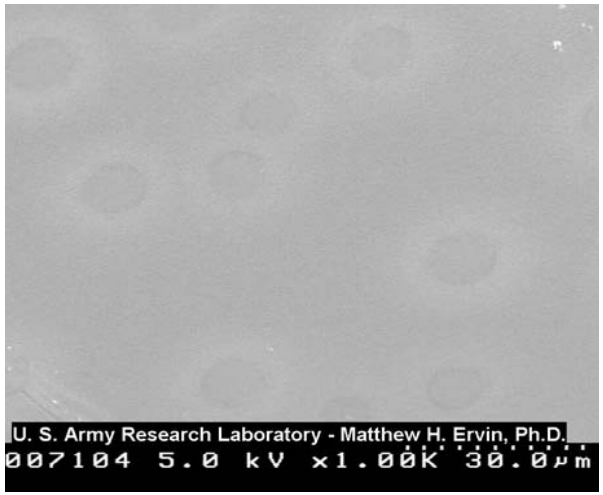
Strained wafer as measured by Laser Light Scan



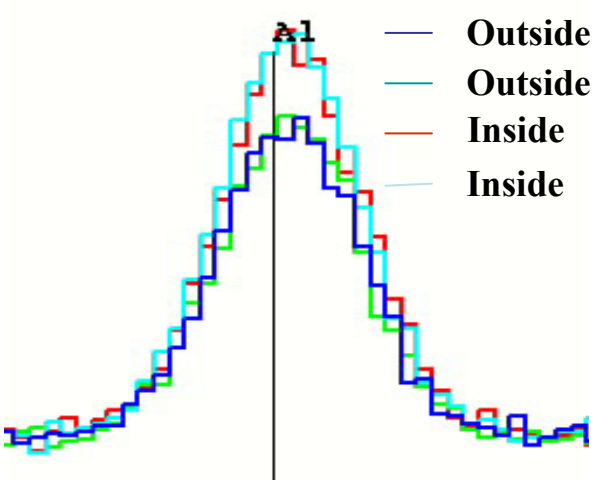
Oxygen contamination during Fe doping as determined from SIMS

1. Contractor had high breakage in their wafers.
2. Our laser light scan showed that the wafer was highly strained.
3. They grew thicker buffer to accommodate mismatch.
4. Contractor had problem doping buffer with Fe to increase its resistance.
5. Our SIMS measurement showed O impurities.
6. Oscillations in oxygen concentration provided insight into source of contamination.

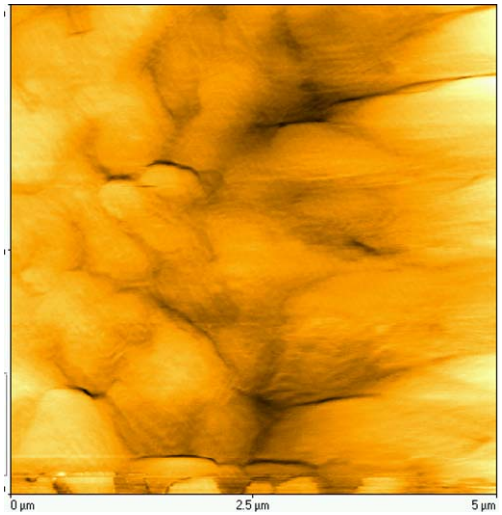
Growth of Device Structures



SEM shows 'spots'



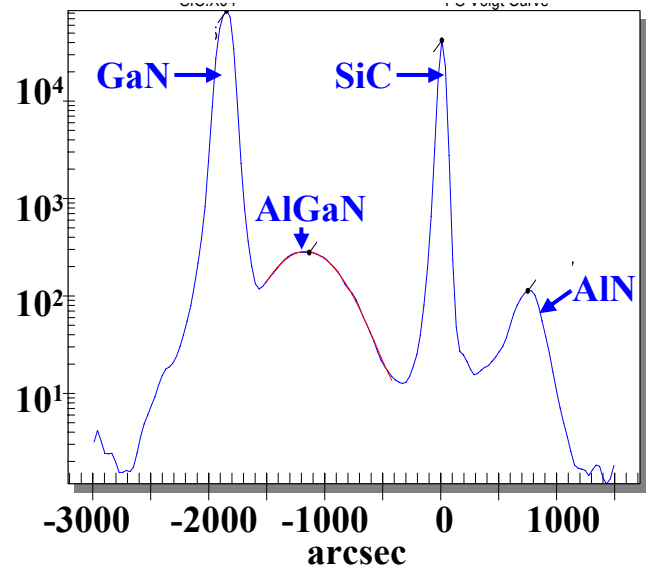
EDAX inside and outside of the 'spots'

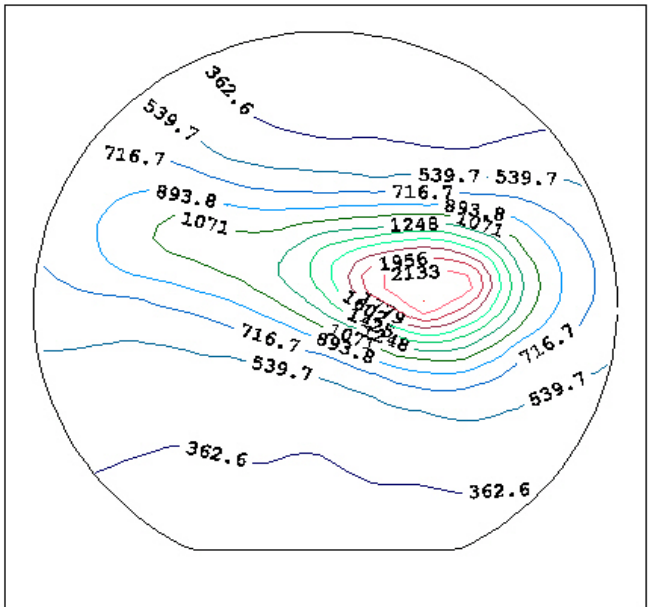


AFM of region surrounding the spots

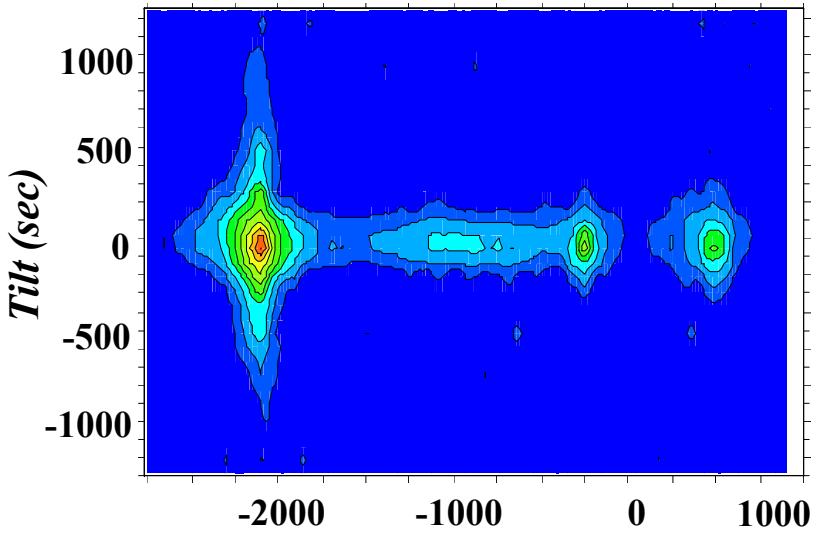
1. DARPA contractor was having poor device yields.
2. Our SEM analysis of the AlGaN indicated segregation.
3. Our EDAX analysis showed more Al inside than outside of the 'spot'.
4. Our AFM analysis showed three dimensional growth in region outside of 'spot' producing a rough surface.
5. Concluded that growth temperature for AlGaN too low.
6. Contractor fixed thermocouple and increased yield.

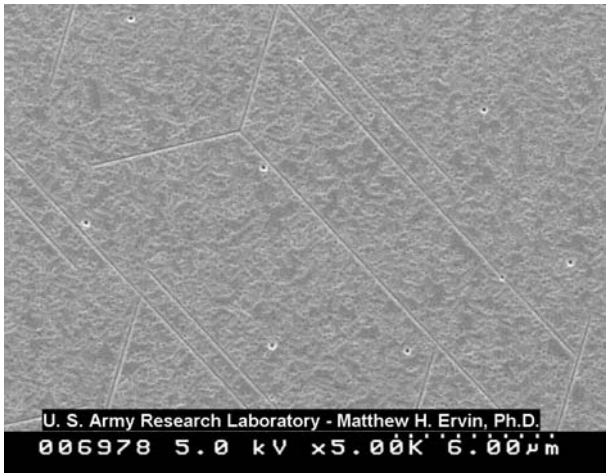
Growth of Device Structures





Sheet Resistance Map

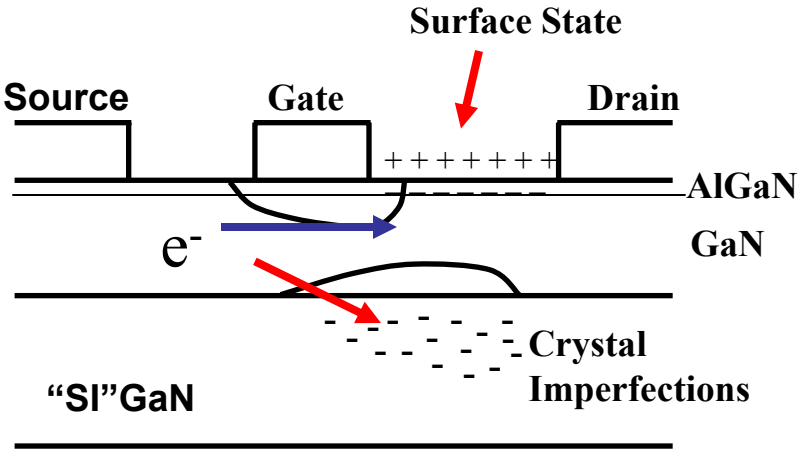




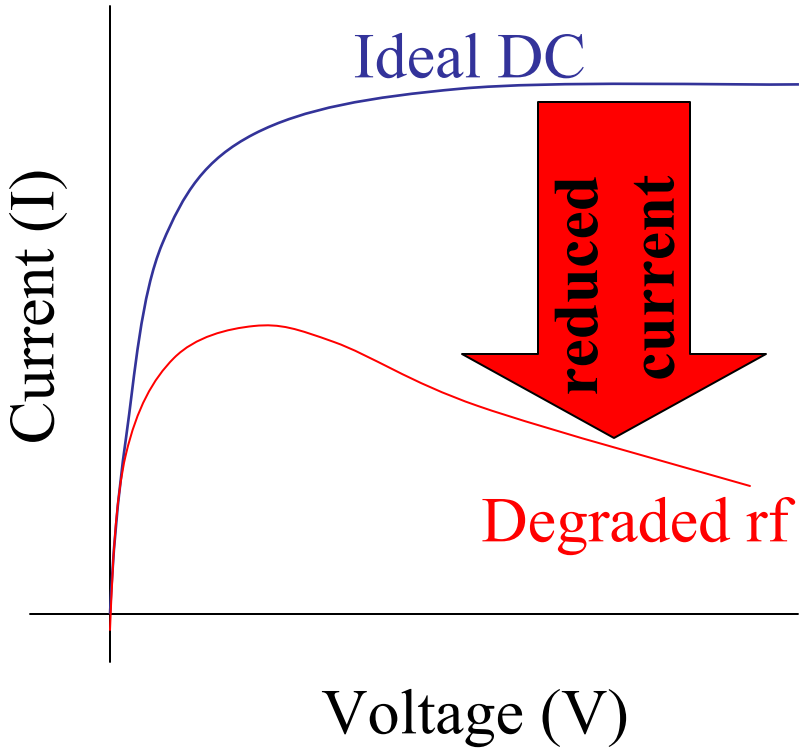
SEM of AlGaN Surface

1. Sheet resistance map shows high resistance regions.
2. X-ray Θ-2Θ shows large Al concentration.
3. Reciprocal lattice map confirms high strain.
4. SEM shows cleavage cracks.
5. Recently cracks at gate on drain side detected when larger voltage is applied.
6. Speculate this is due to piezo-strain.
7. Highest electric fields at the gate on the drain side.

Current Collapse in HEMTs



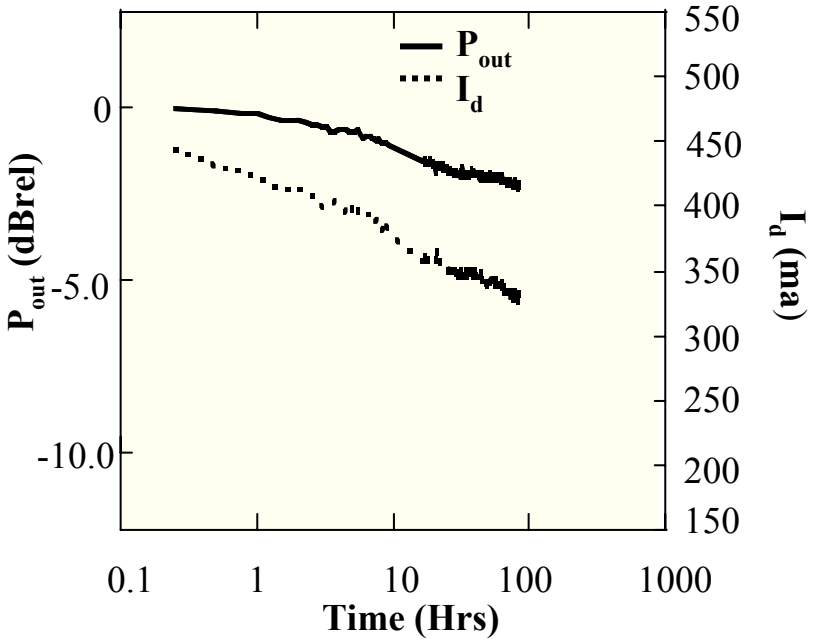
Crystal imperfections or surface states "trap" electrons and degrade RF current flow



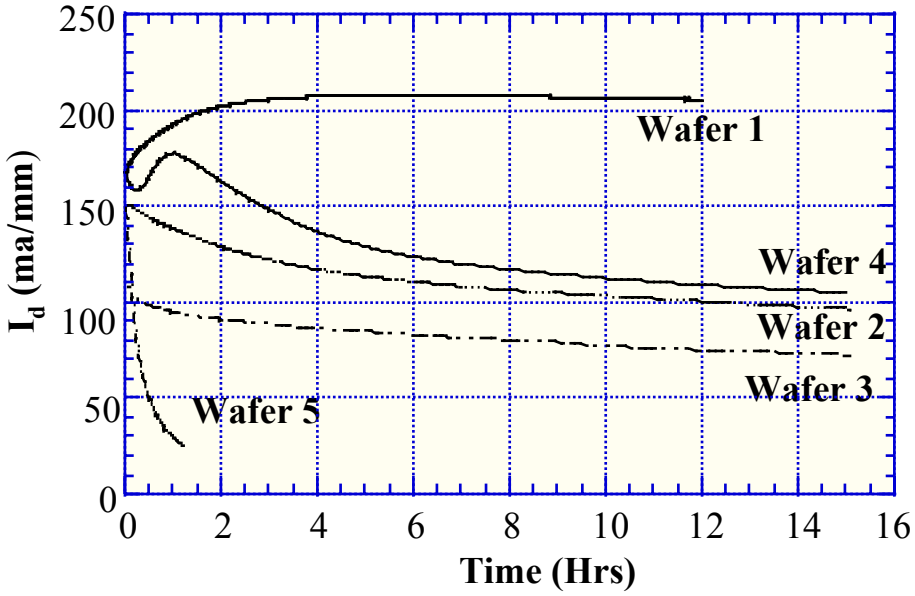
Buffer traps determined by epitaxial growth conditions. Strong polarization induced surface effect is minimized by silicon nitride passivation.

Poor HEMT Reliability Due to Defects?

RF reliability
Power (solid) and Drain Current (dashed)



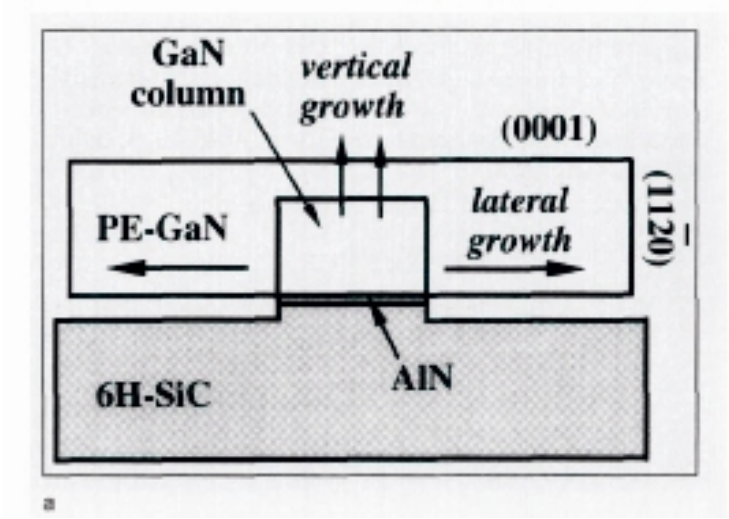
DC stress of multiple wafers



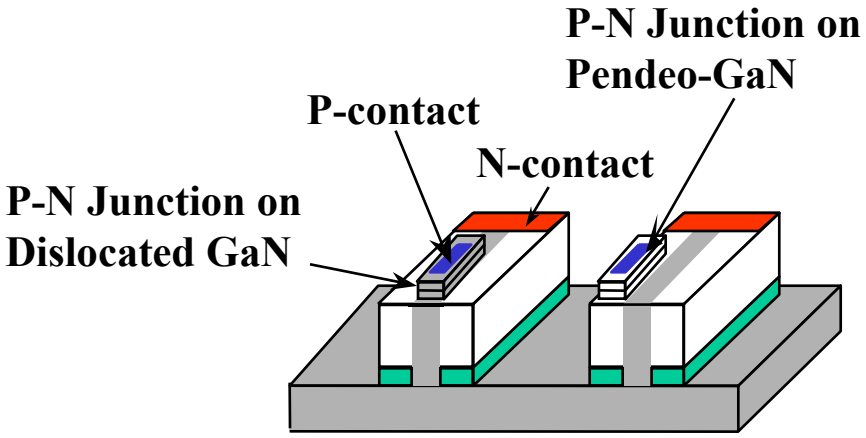
1. Decrease in drain current follows degradation in output power
2. Devices degrade with DC stress as well; degradation varies from wafer to wafer and on same wafer
3. Reliability of device can depend on the method used to grow it.

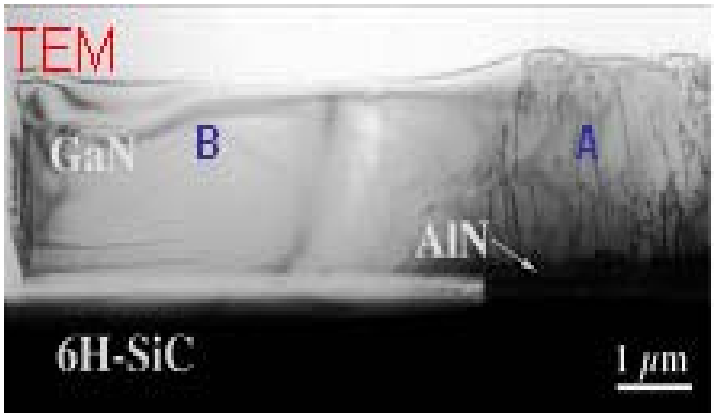
Wafer 1: Epi source 2 - MOCVD
Wafer 3: Epi source 1 - MBE
Wafer 4: Epi source 2 - MOCVD
Wafer 5: Epi source 1 - MBE

Study Effects of Defects Using Pendeo-Epitaxial Grown Device Structures

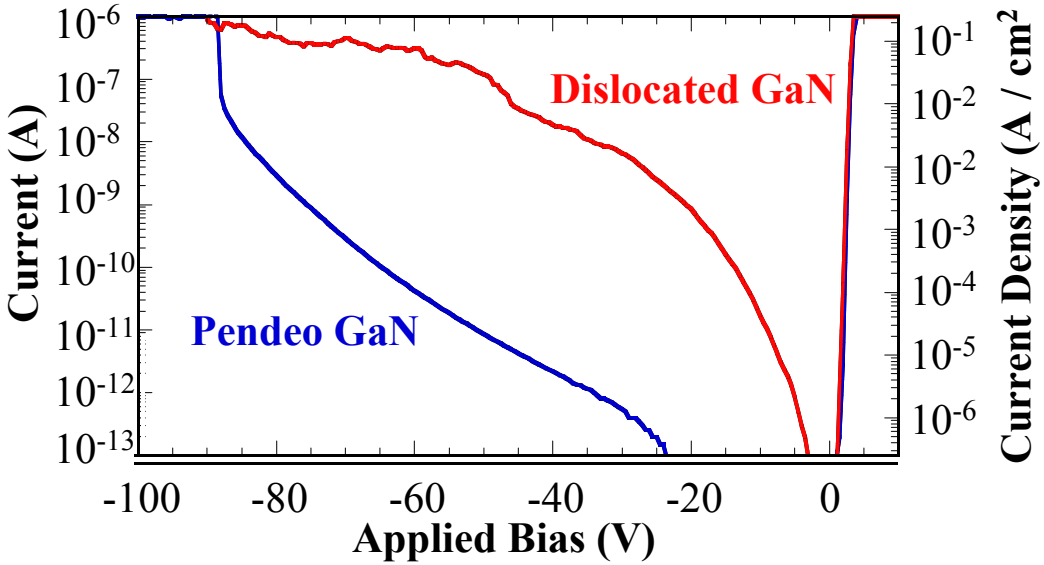


Schematic of Pendeo-Epitaxy Growth



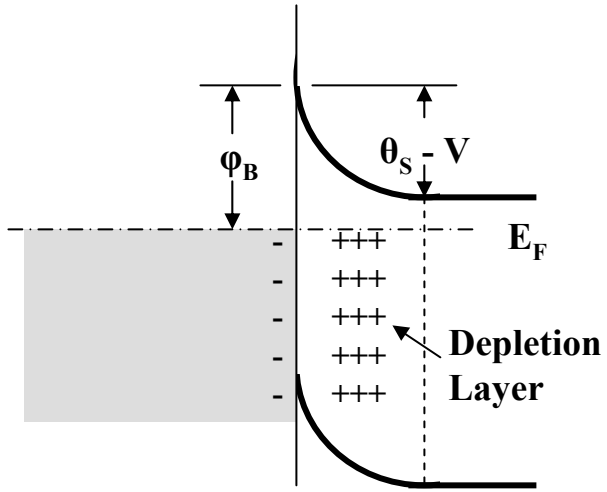


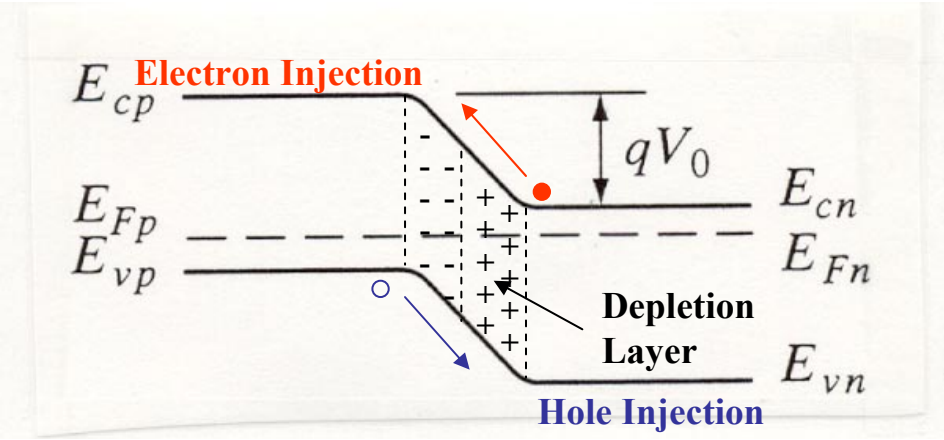
Pendeo material has fewer dislocations



'Gate' Leakage Current

SiC Schottky and PN Diodes





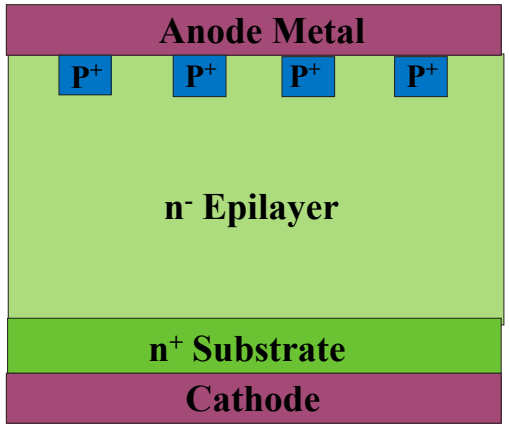
SCHOTTKY DIODE

1. Many electrons injected from semiconductor into the metal under forward bias, virtually none under reverse bias.
2. There are no holes so there is no minority carrier injection. No EHP recombination so faster and no stacking fault generation.
3. Depletion layer narrower under forward bias, wider under reverse bias.
4. Poor quality interface allows for large leakage current under reverse bias.

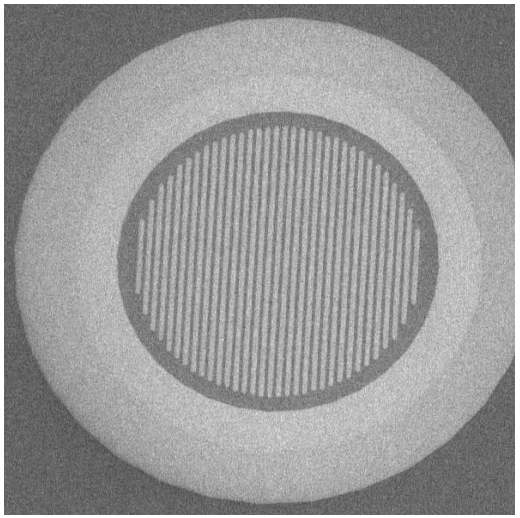
PN DIODE

1. Many electrons injected into p-type material and many holes injected into n-type material.
2. There is minority carrier injection under forward bias that have to recombine, and this takes time, which slows the device down.
3. The energy produced by EHP recombination can produce stacking faults, which cause drift in the forward bias characteristics.
4. Depletion layer narrower under forward bias, wider under reverse bias.

The JBS Diode



Schematic of Side View



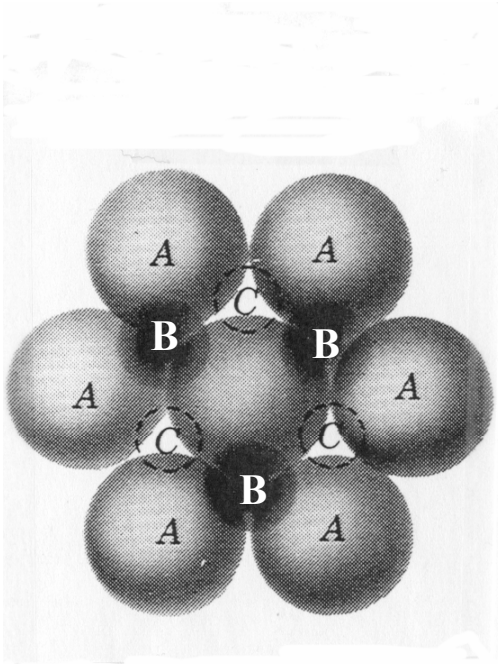
Top View of an Implanted Device

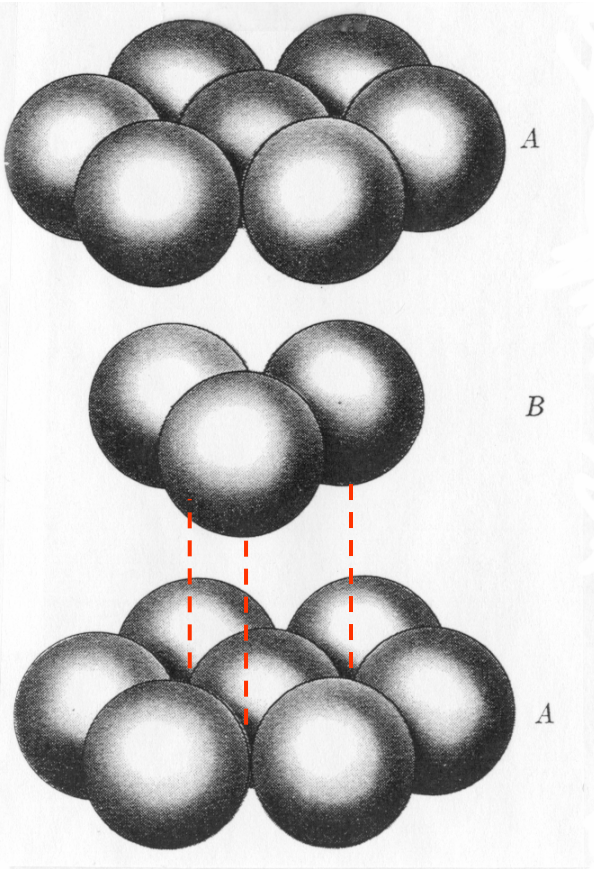
JBS DIODE FABRICATION ISSUES

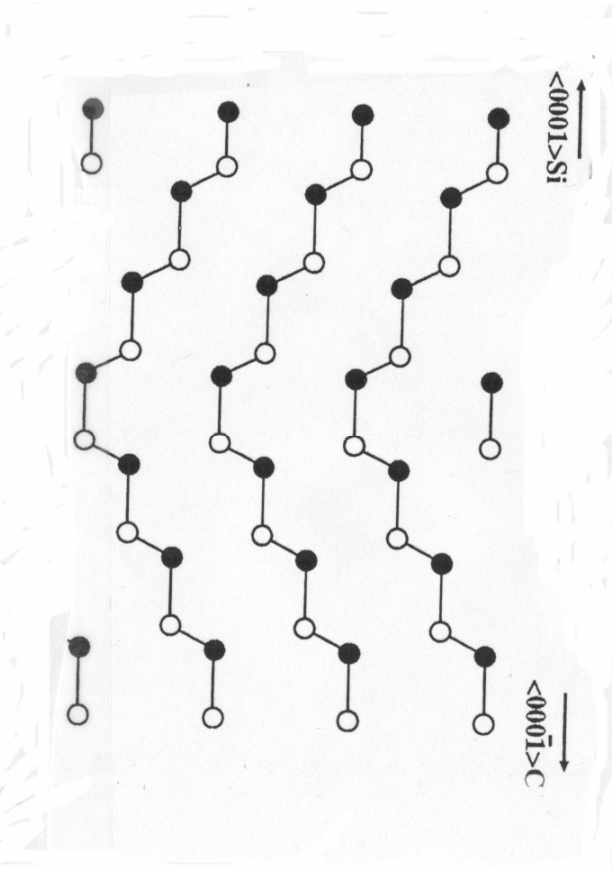
1. The JBS diode behaves like a Schottky diode under forward bias. The voltage across the junction is too low to 'turn on' the P^+n^- diode.
2. The JBS diode behaves like a PN diode in reverse bias because the depletion layers from the P^+ layers block the flow to the Schottky metal.
3. The P channels are formed by ion implantation.
4. The damage created by the implant process has to be annealed out to activate the implanted ions.
5. At the temperature required to anneal out the implant damage, the silicon evaporates preferentially and damages the device.
6. We developed a BN/AlN annealing cap that blocks the silicon evaporation and can be removed after the anneal without harming the device.

SiC Polytypes

SiC has over 200 polytypes - hard to grow the one you want!

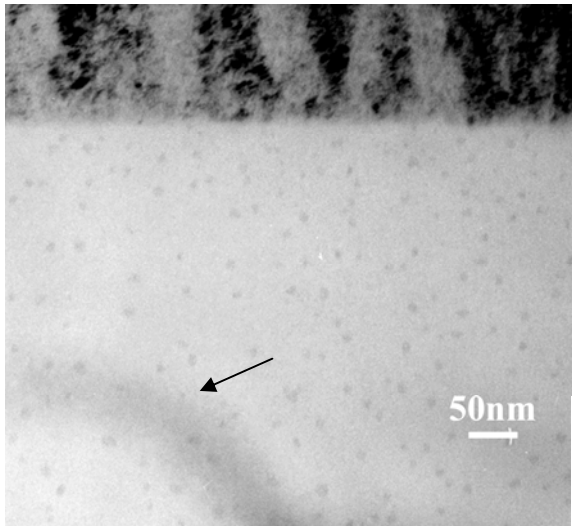




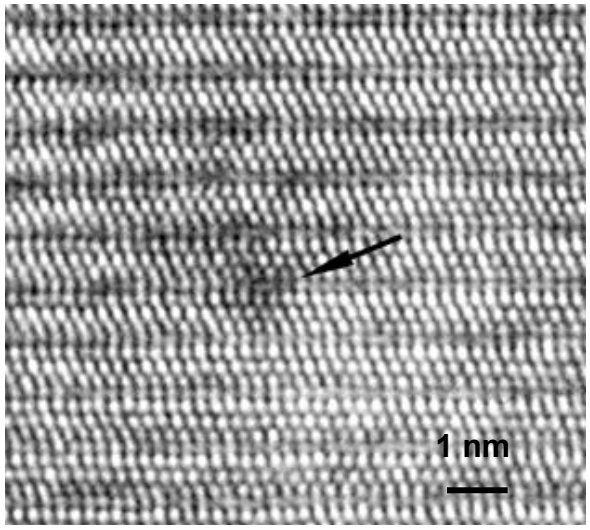


3C **2H** **6H**

Persistent Ion Implanted Defects

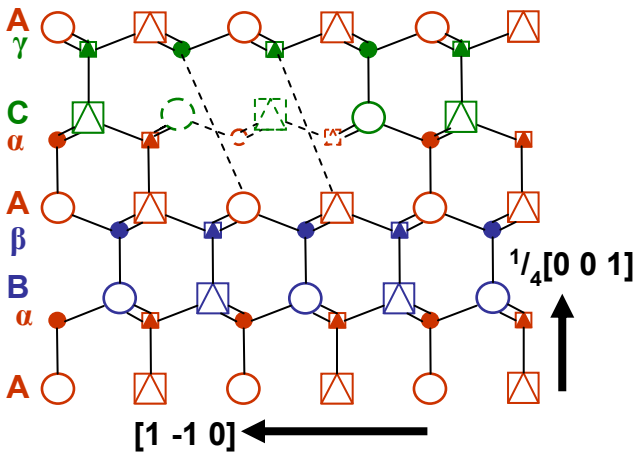


TEM Showing Defects (spots)

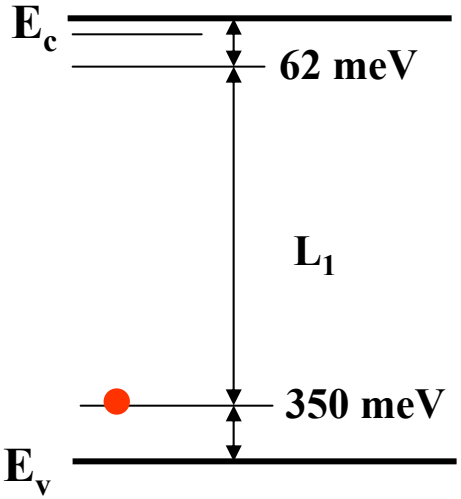


HRTEM of Spots Showing SF

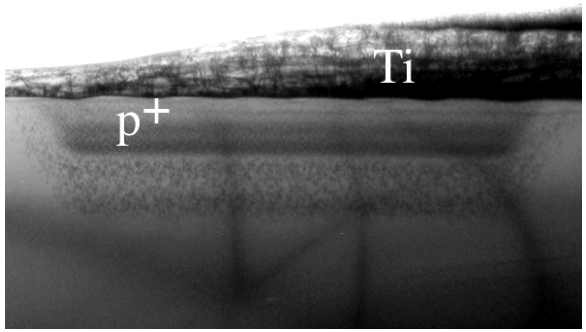
1. TEM shows that annealed ion implanted region contains persistent defects; HRTEM show that defects are stacking faults.
2. Defects thought to be a Frank intrinsic stacking fault can be formed by the condensation of divacancies; has energy states in energy gap associated with it.
3. Solution is to reduce implant dose near junction.



Schematic of Frank intrinsic SF formed by the condensation of divacancies.

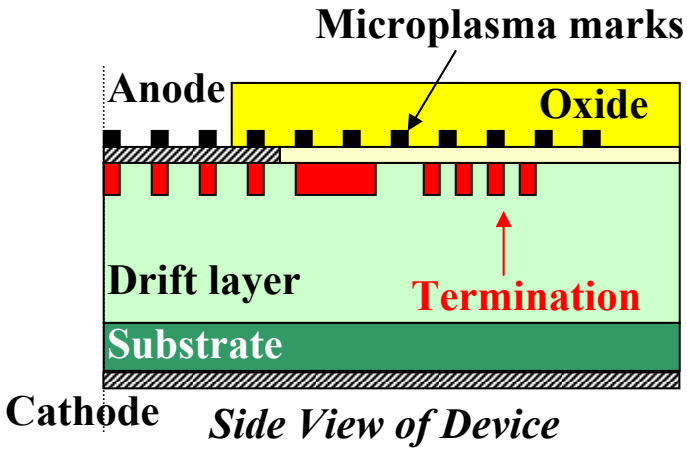


Janzen, et al theory that defect is a deep donor



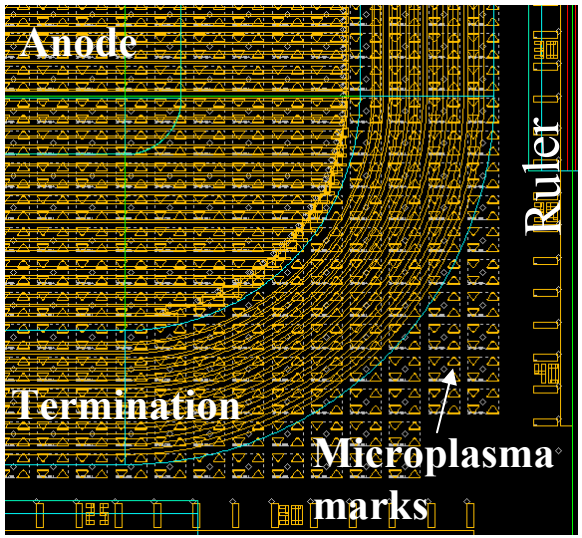
High/Low, Shallow/Deep Implantation Dose

Premature Breakdown in Implanted Guard Rings

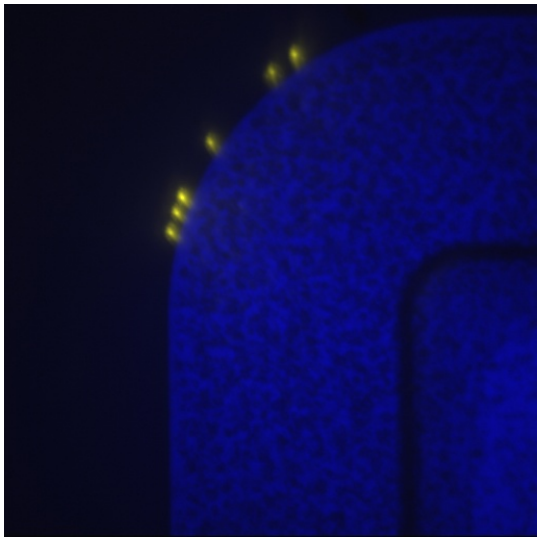


Side View of Device and Guard Rings

1. Guard rings are necessary to prevent premature breakdown at the edges.
2. Guard rings are implanted.
3. There is a possibility of premature breakdown caused by the persistent defects caused by ion implantation.

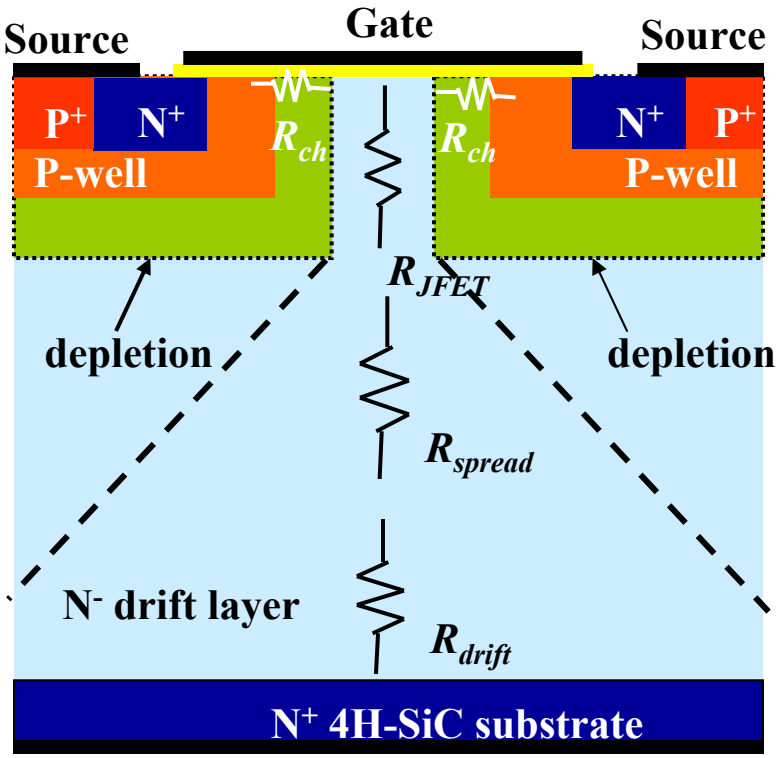


Top View of Device and Guard Rings



Top View of Device with Microplasmas

SiC DMOSFET

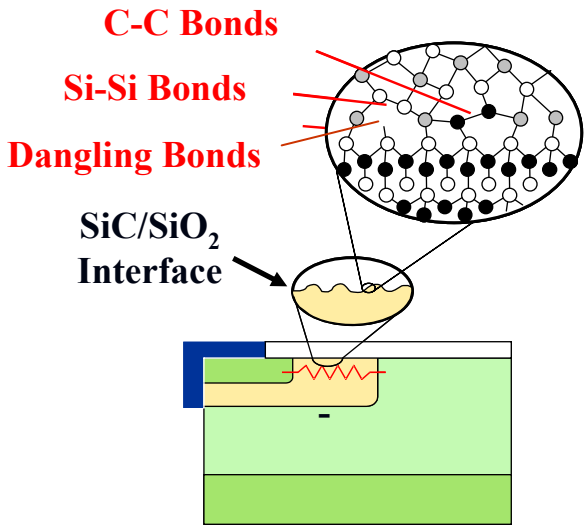


Conventional 4H-SiC DMOSFET

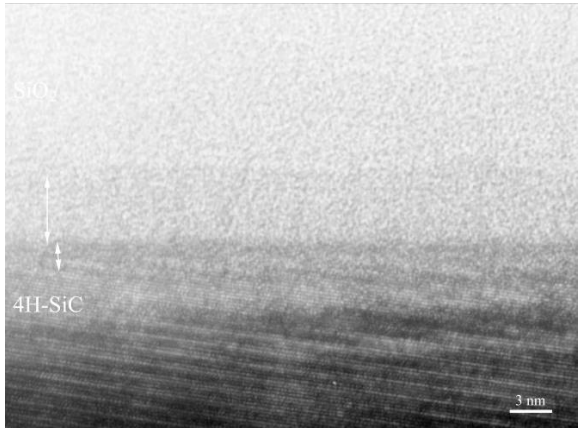
R_{Ch}	9.8 μΩ cm^2
R_{JFET}	8.2 μΩ cm^2
R_{drift}	3.4 μΩ cm^2
R_{spread}	3.7 μΩ cm^2
R_{Other}	1.0 μΩ cm^2
$R_{sp.on}$	26.1 μΩ cm^2

μ_{eff} (channel) = 15 cm^2/V·s
μ_{bulk}=600 cm^2/V·s)

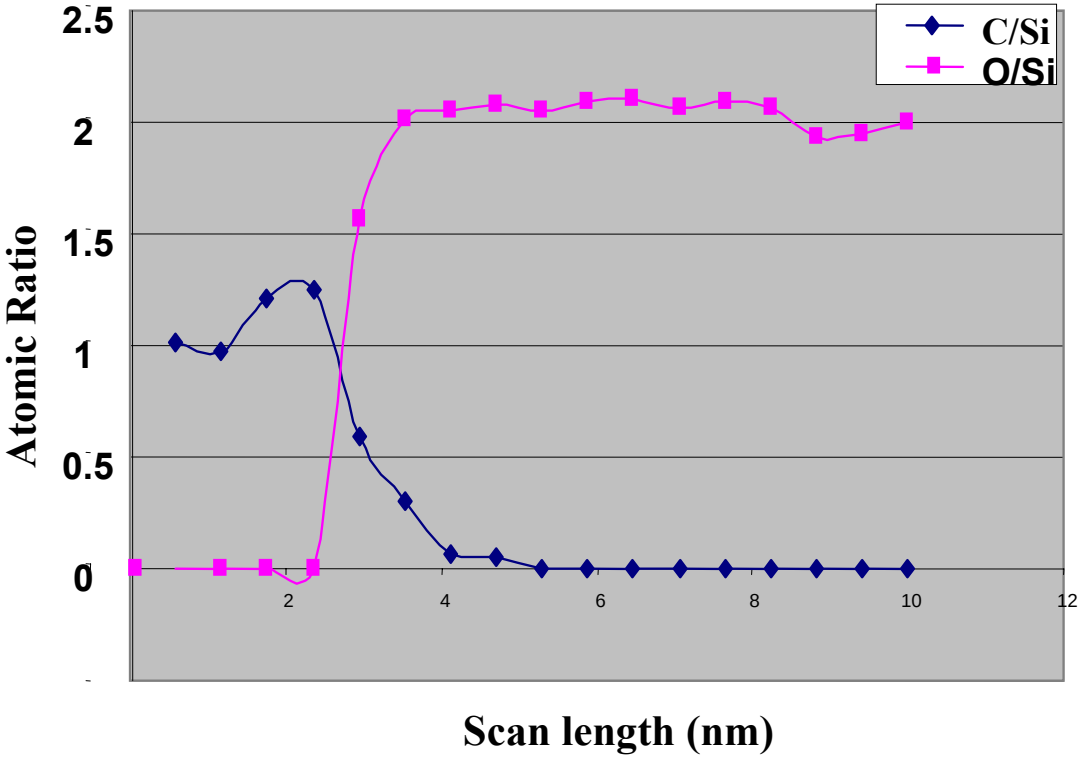
Possible C-Contamination of the Oxide



Schematic of the SiC/SiO_2 Interface



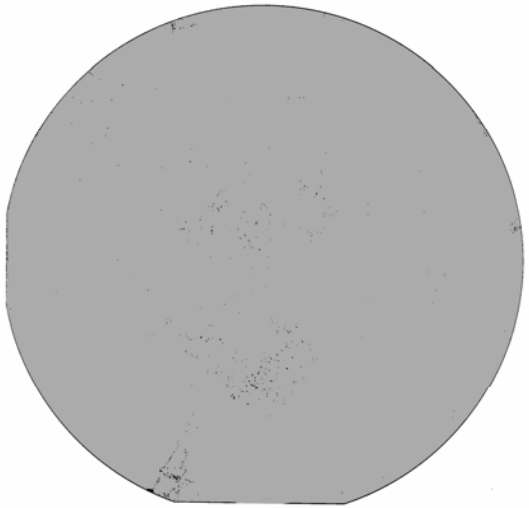
HRTEM of the SiC/SiO_2 Interface

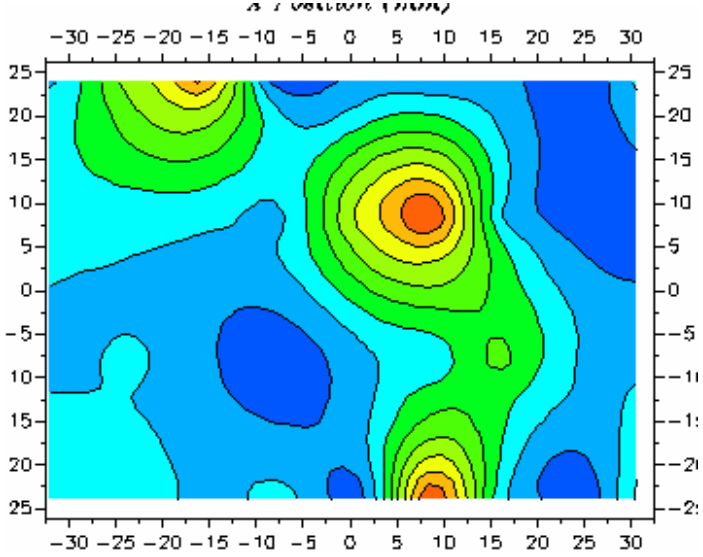


There is evidence from EELs of increased C/Si ratio on both side of the interface consistent with Si vacancies in SiC (SDR studies) and also C incorporation in the oxide transition layer

Cradle to Grave Materials – Device Correlation

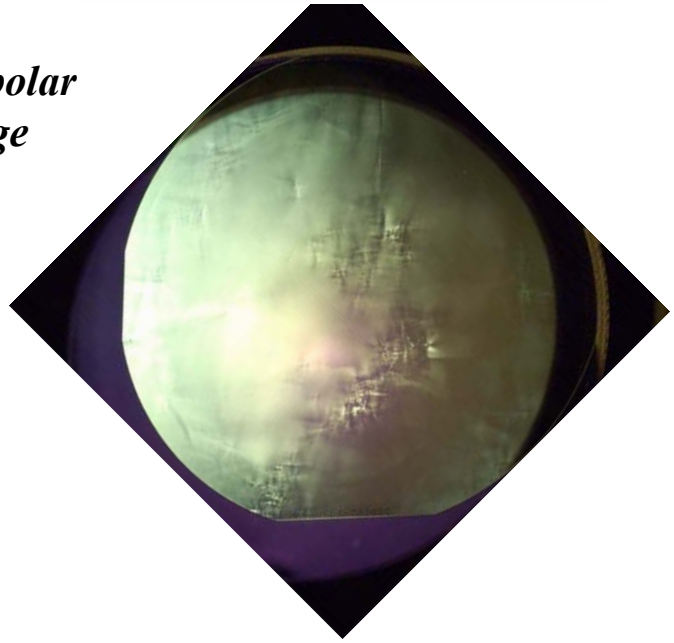
Etch pit density map

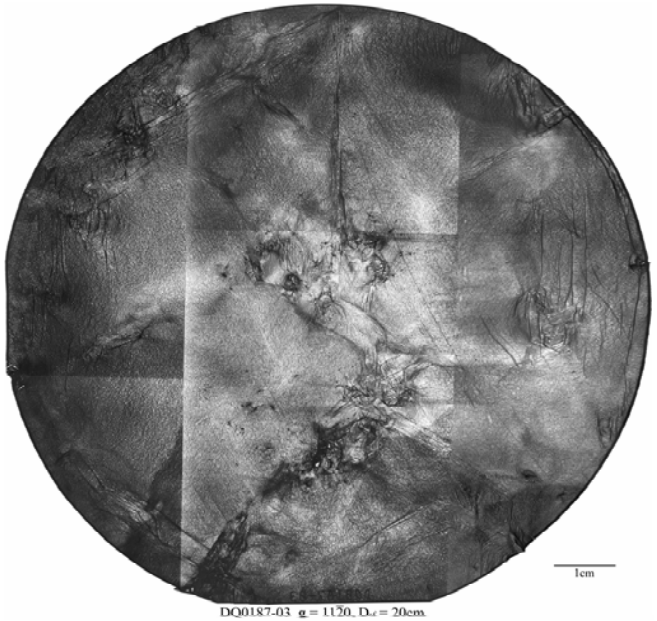




X-ray rocking curve map

Cross polar image





Synchrotron X-ray topograph

Conclusions

GaN/AlGaN HEMT

1. Crystalline defects will be a major cause of degraded device properties, reduced yield and reliability, and premature failure until a GaN substrate can be prepared.
2. A more quantitative understanding of the effects of defects on the device so that we will be better able to engineer short term solutions.
3. One way this can be accomplished is to compare HEMTs made from pendeo-epitaxial grown structures with those made from structures grown the usual way.

SiC DEVICES

1. The JBS diode has persistent ion implant induced defects that cannot be removed. Devices can be engineered to reduce their effects by reducing the dose in the vicinity of the p-n junction. Regrown P^+ channels should also be considered.
2. The critical issue with SiC MOSFETs is the low channel mobility. TEM studies have shown that one of the issues could be excess carbon in the oxide near the interface.
3. A comprehensive study of the effects of the crystalline defects in the original wafer should provide cost effective ways for improving the SiC devices fabricated from them.